D3.7. Final WP3 scientific report

WP3 – Smart Energy Distribution, Microgrids and Grid of Microgrids

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List of abbreviations

BEN	Beneficiary
CAU	Christian-Albrechts-Universitaet Zu Kiel
CF-MAB	Current-Fed Multi-Active Bridge
CNTU	Chernihiv Polytechnic National University
DAB	Dual active bridge
Dn	Deliverable (number)
DoA	Description of Action
DS	Doctoral School
ER	Energy Router
ESR	Early Stage Researcher
ETN	European Training Network
GA	Grant Agreement
GUT	Politechnika Gdanska
IRP	Individual Research Project
ITN	Innovative Training Network
KIT	Karlsruhe Institut für Technologie
MMC	Modular Multilevel Converter
MSn	Milestone (number)
MSCA	Marie Sklodowska-Curie Actions
PC	Project Coordinator
REC	Research Ethics Committee
RSC	Recruitment and Secondment Committee
USA	University of Salerno
WPn	Work Package (number)

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1. Executive summary

The present deliverable provides the final report about the scientific activities done and main results obtained in ***Work Package 3-Smart energy Distribution. Microgrids and grid of microgrids***. The main objectives of WP3 are to explore the possibilities of microgrids for energy management to address the challenges of secure energy routing and power quality control, as well as advanced distribution grid management and the use of radial grids. The innovative results provided by the ESRs are aimed to identify and demonstrate new ways of collaborative distributing electric energy and new operation strategies as well as operating in connected and islanding modes; to design converters and strategies to control microgrids (as optimal operational parts of distribution grids) to manage energy flows and minimize transportation losses; to coordinate the production of different generators with the consumption of different consumers to match generation and consumption in a safety and optimize way; finally to analyse the new opportunities of storage system in microgrids and conventional grids.

The first research activity, carried out by ESR05 and coordinated by CNTU unit, has been concentrated on the design and control of an advanced Energy Router (ER) architecture for hybrid microgrids, enabling coordinated integration of photovoltaic systems, battery storage systems, AC/DC loads, and grid interaction through a unified power electronic interface. This solution aims to improve energy flow management, enhance operational flexibility under both grid-connected and island conditions, and contribute to more efficient and resilient microgrid operation. The main results in this research area consist into the design and experimental validation of a 5kW multiport converter, including a single-phase AC input, single-phase AC output, photovoltaic input, battery storage interface, and isolated DC-grid output terminals. Reliability and protection aspects of the proposed architecture, including safety considerations and protection strategies for hybrid microgrid operation, as well as the control strategies under dynamic conditions, to enhance the reliability and dynamic performance of the multiport energy router has been also considered.

The second research area, covered by ESR06 and coordinated by GUT unit, concerned the development of a new power electronics facilities for energy transfer system with improved efficiency and power density and analyse future energy system including wireless charge system for electric vehicles. The proposed multiport Current-Fed Multi-Active Bridge (CF-MAB) converter topology allows optimization of power distribution among system components (BT, EVs and the LV DC traction grid), reducing losses and improving DC grid power quality. The analysis of the CF-MAB converter modulation techniques has shown that the default single-phase shift (SPS) modulation results in increased transformer RMS currents and reduced efficiency. Moreover the developed high-level converter control algorithm enables the utilization of EV batteries and an additional storage battery as flexible components of a smart grid by providing bidirectional charging as well as V2G and V2V operation. The system enhances the power quality of a low-voltage DC grid by providing grid voltage stabilization, optimized power flow among system participants and improved efficiency through the recuperation of traction transport braking energy. Experimental verification, conducted using a smaller-scale converter prototype, demonstrated its ability to independently deliver power to any port without affecting the power of other ports.

The third reserch pillar, involved ESR07 and coordinated by CAU unit, is focused on the development of a Real-Time Model-Assisted Modular Multilevel Converter (MMC) Emulator. This test bench integrates an actual MMC submodule (SM) with a fully detailed real-time model of the MMC running on a real-time simulator. The hybrid setup enables safe, accurate, and flexible investigation of complex test cases such as AC/DC faults, overcurrent conditions, and submodule failures, which are difficult, expensive, or dangerous to reproduce in full-scale or even scaled-down laboratory prototypes. Moreover, the presence of real hardware in the loop makes this setup particularly valuable, as it allows the evaluation of the converter real world behaviour under conditions that closely replicate practical operating scenarios, ensuring highly realistic and reliable hardware-validation results. These studies explored converter control strategies, submodule hardware validation, and real-time simulation methods for advanced power electronic systems. The Power Electronics Laboratory at CAU, equipped with OPAL-RT real-time simulator and small-scale MMC prototype hardware, provided the experimental infrastructure necessary to validate the concept and gather representative results.

The final research activity, conducted by ESR08 and coordinated by KIT, is structured in two phases. This follows the departure of the initially appointed researcher from the SMARTGYsum consortium midway through the project (late 2024). After a new recruitment call, a second researcher was hired for the ESR08 position. Despite

minor adjustments made to reflect their different background, both researchers adhered to the IRP8 to ensure the successful achievement of the project's objectives.

The first ESR08 conducted his **research mainly focused on DC networks, addressing several aspects: a comparison between isolated and non-isolated converter topologies in terms of efficiency and short-circuit behaviour; the modelling of a dual active bridge (DAB) converter through different integration techniques to assess their impact on the accuracy of power electronic simulations; and a comprehensive review of DC fast-charging stations, covering standards, isolation schemes, microgrid architectures, voltage and power levels, battery energy storage systems, and power converters.** The study of an 8 kW DAB converter operating over a wide output voltage range by using a bidirectional DC power supply as active load to simulate the behavior of an EV battery has been part of the research task. The DAB prototype has been developed in the KIT Energy lab 2.0 by using commercial hardware provided by Imperix to verify its applicability in DC fast charging applications for electric vehicles (EVs).

Building on the DC network expertise developed in the first phase, the second ESR08 **shifts his research focus towards hydrogen-based energy systems, investigating the techno-economic feasibility of hydrogen-based energy storage (HES) integrated with photovoltaic (PV) generation in off-grid microgrids. This phase lays the economic and technical foundation for subsequent stages, which will include dynamic modelling in MATLAB/Simulink, development of control strategies, and experimental validation using the Power Hardware-in-the-Loop (PHIL) infrastructure of the H2-in-the-Loop (H2IL) facility at KIT Energy Lab 2.0. A dedicated MATLAB toolchain was developed to automate system sizing and economic assessment, designed to be replicable across different geographic locations and enabling a comparative feasibility assessment across diverse irradiance conditions in Europe.**

1.1. Objectives of the deliverable

The objective of this deliverable is to collect the results obtained in the corresponding IRPs included in WP3. The research work carried out by each ESR is reported in the section identified by the corresponding IRP project:

- IRP05 – Energy Router for Hybrid Microgrids for efficient and robust energy and power management
- IRP06 – EV chargers, developing an active bidirectional charger able to provide anciallary services
- IRP07 – Reliability and availability of Smart Transformers for cost effective and high quality of services in the grid
- IRP08 – Real-time modelling and validation of Distributed Energy Storage Systems and Integration strategies

1.2. Organisation of the deliverable

The present deliverable is organised in five sections. Sections 1 and 2 give a general overview of WP3 research activities. Section 3 describes the main results of WP3 research tasks, it is composed of 4 subsections that collects the progress made by the ESRs with their results and outcomes. This section shows the main WP3 contributions in terms of scientific results and practical application of ESRs research activities. In subsection 3.1 is reported the ESR05 activity that is devoted to study and development of Energy Routers for Hybrid Microgrids enhancing efficiency and robustness. ESR06 activity is reported in subsection 3.2 and raises to the development of an Active Bidirectional Energy Charger for providing Ancillary Services. The work of ESR07 is reported in subsection 3.3 dealing to the research on the reliability of smart transformers to ensure cost-effective and high-quality services. ESR08 activity is reported in subsection 3.4 and refers to real time modelling of power converters for energy storage system technologies with low computation effort and investigation of new opportunities of storage system in microgrids and conventional grids. The report includes also Sections 4 and 5 respectively devoted to WP3 final conclusions and references.

2. General progress of the action

2.1. WP3 Objectives and tasks

WP3 (Smart Energy Distribution, Microgrids and Grid of Microgrids) objectives are:

i. To identify and demonstrate new ways of collaborative distributing electric energy and new operation strategies as well as operating in connected and islanding modes;
ii. To design converters and strategies to control microgrids (as optimal operational parts of distribution grids) to manage energy flows and minimize transportation losses.
iii. To coordinate the production of different generators with the consumption of different consumers to match generation and consumption in a safety and optimize way
iv. To analyse the new opportunities of storage system in microgrids and conventional grids

WP3 (Smart Energy Distribution, Microgrids and Grid of Microgrids) tasks are:

- Task 3.1: Development of Energy Routers for Hybrid Microgrids enhancing efficiency and robustness (USA-CNTU).
- Task 3.2: Development of an Active Bidirectional Energy Charger for providing Ancillary Services. (USA-GUT).
- Task 3.3: Research on the reliability of smart transformers to ensure cost-effective and high-quality services. (USA-CAU).
- Task 3.4: Real time modelling of energy storage system technologies with low computation effort (KIT-OPAL).
- Task 3.4: Elaboration of partial and final scientific reports on Smart Energy Distribution (USA).

2.2. WP3 – Workpackage progress

ESR	Starting date	General evaluation	Status
5	01/08/2022	ESR05, Mohammadreza Azizi has successfully completed his research work, and all major deliverables have been achieved. The designed system fully aligns with the objectives of developing efficient and robust power electronics solutions for intelligent energy management in microgrids and residential applications. No major deviations occurred. The project successfully delivered a functional single-cell three-phase energy router prototype, achieving high dynamic performance, safety, and flexibility, meeting the intended research and development objectives. In conclusion, all main tasks in accordance with the Personal Career Development Plan were successfully carried out. PhD thesis (cotutelle agreement between Chernihiv Polytechnic National University and University of Extremadura) was successfully defended 06.02.2026.	IRP completed PhD thesis defended
6	1/06/2022	ESR06, Mykola Lukianov carried out his research workflow: from conceptual development to the realization of a small-scale hardware prototype of the bidirectional multi-terminal EV charging station. EV charger prototype has been finished. Currently ESR06 is a PhD student at GUT, he is writing the thesis dissertation, with the final defense expected by October 2026.	IRP completed PhD thesis defended planned
7	1/08/2022	ESR07, Mahyar Hassanifar, successfully carried out his research and studies on the defined tasks and topics at the Chair of Power Electronics, Kiel University. His work primarily focused on the investigation and	IRP completed PhD

		development of control strategies with particular emphasis on the control of insertion and charging of redundant submodules (SMs) for Modular Multilevel Converters (MMCs). In parallel, he developed a hardware test bench specifically tailored for experimental validation, enabling the testing and analysis of various MMC control scenarios under realistic operating conditions. The developed setup provides a flexible platform for evaluating converter behavior, assessing dynamic performance, and verifying the effectiveness of the proposed control approaches. The outcomes of this work have been presented through conference presentations and journal publications, in alignment with the overall research objectives of the project. The obtained results and conducted research were well-aligned with the defined goals in the work package. ESR07 registered as a Ph. D. student at the CAU and the Ph. D. studies are still in progress.	in progress
8	1/04/2022	ESR08, Gabriele Arena, performed extensive review studies on DC applications, in particular on electric vehicle fast-charging stations. These studies were carried out together with the TalTech group, and a journal contribution has been published. As a follow-up work, an experimental setup for flexible electric vehicle fast-charging stations has been designed and assembled at the KIT. He targeted a re-configurable 400V/800V system, that was able to achieve high efficiency across the full voltage range. The next step would have been to model this system in a real time simulator and validate the results with the developed setup. Mr. Arena withdrew from the PhD program at the end of 2024 to pursue a career in industry as a software developer, a role he currently holds.	On-time with the IRP. Terminated.
8	2/04/2025	ESR08, Danilo Di Berardino, is currently taking over the modelling and business plan tasks of Mr. Arena with a slightly modified focus. He is developing scenarios for integration of DC Hydrogen in micro- and off-grids, focusing on the technical and economic feasibility. Mr. Di Berardino performed a cost analysis of the single hydrogen components, considered the provision of services to the grid, and analyzed the return of investment for hydrogen storage plants. Currently, a specific off-grid scenario has been chosen, and he is going to implement it in a real time simulator. The next step will entail the validation of the model with the hydrogen experimental plant at KIT "H2-in-the-loop" and the development of control algorithms for grid services provision.	On-going IRP and PhD

3. WP3 Tasks results

3.1. Task 3.1 – IRP5 "Energy Router for Hybrid Microgrids for efficient and robust energy and power management"

3.1.1. Introduction

The increasing penetration of distributed renewable energy sources and energy storage systems has significantly accelerated the development of hybrid AC/DC microgrids. These systems require advanced power electronic interfaces and intelligent control strategies to ensure efficient energy distribution, reliable operation, and coordinated power management among multiple sources and loads. Within this context, the concept of the Energy Router (ER) has emerged as a promising solution to flexibly interconnect different energy resources, storage systems, and loads while enabling efficient power exchange between local microgrids and the utility grid. Researchers have already proposed various topologies and control strategies for ER; however, there are still research gaps and challenges that should be addressed. Safety and protection issues and the control response in dynamic conditions are among these challenges.

In line with the objectives of WP3 – Smart Energy Distribution, the **task 3.1** focuses on the design and control of an advanced ER architecture for hybrid microgrids, enabling coordinated integration of photovoltaic systems, battery storage systems, AC/DC loads, and grid interaction through a unified power electronic interface. This solution aims to improve energy flow management, enhance operational flexibility under both grid-connected and island conditions, and contribute to more efficient and resilient microgrid operation. Under umbrella of this task, the following main research sub-tasks were addressed:

1. Design of a 5 kW multiport converter, including a single-phase AC input, single-phase AC output, photovoltaic input, battery storage interface, and isolated DC-grid output terminals.

2. Investigation of reliability and protection aspects of the proposed architecture, including safety considerations and protection strategies for hybrid microgrid operation.

3. Improvement of the control system under dynamic conditions, to enhance the reliability and dynamic performance of the multiport energy router.

During the doctoral research, the scientific activities were carried out by ESR05 Mohammadreza Azizi across several institutions within the SmartGYsum network. The work officially started on 1 August 2022, when the initial literature review and preliminary studies on hybrid microgrids and ER concepts were conducted partly through remote collaboration and partly during a short research stay in Turkey under the remote supervision of Dr. Oleksandr Velihorskyi and Dr. Oleksandr Husev (CPNU).
From March 2023 to 31 July 2025, in accordance with the collaborative agreement between CPNU and the University of Extremadura (UEX), and under the order of CPNU on academic mobility to the University of Extremadura (Spain), UEX served as the main host institution, where the majority of the research activities were performed. During this period, the research progressed from theoretical investigations and system modeling to detailed simulation studies, leading to the design and development of the proposed ER architecture.
In addition, three secondment periods were completed at Gdańsk University of Technology (Poland) as part of the doctoral training program. The first secondment took place from 1st November to 31st December 2023, focusing on safety aspects, grounding strategies, and, in particular, the analysis and mitigation of DC leakage currents at hybrid microgrid interfaces. The second secondment, conducted from 10th May to 9th July 2024, concentrated on improving the control strategy under dynamic conditions, including the development and simulation of a Flatness-Based Control (FBC) approach. The third secondment, carried out from 1st April to 30th June 2025, was dedicated to testing the proposed architecture and evaluating system performance under different operational scenarios and dynamic conditions.

Personal contribution of the applicant that the ESR directly carried out:

– Reviewing the existing structure of ERs and analyzing their performance in different modes and safety conditions.
– Comparative analysis of different isolated dc-dc converters for low-power applications to be used in the overall ER structure.
– Comparative analysis for different scenarios of NZEB connection to the ac grid.
– Development of the simulation model in PLECS software to analyze the open-loop and closed-loop operation, as well as the control system at different levels.
– Studying, modeling and simulating common-ground structures to be used in the general structure of the ER to enhance safety.
– Analyzing and applying modulation techniques for the common-grounded inverter in ERER for an accurate operation in boost, buck and buck-boost modes.
– Reviewing and analyzing dc and ac leakage current and grounding type and configurations in dc and ac systems.
– Analyzing and modeling different scenarios for connecting dc and hybrid NZEB to the ac grid, regarding safety issues in both dc and ac sides.
– Analyzing and simulating dc leakage current in the isolated connection of the ER to ac grid.
– Proposing and tuning the control system based on FBC theory in ER simulation to enhance control response in dynamic conditions.
– Assembling the experimental setup to analyze the general open-loop operation of different parts and converters in the ER system.
– Running experimental tests for different operation modes, including dc-mode, grid-forming, and grid following, as well as dynamic conditions of step changes in loads.

The main outcomes of this research have been disseminated through presentations at several international IEEE conferences. In particular, the main provisions of the dissertation were reported and discussed at four international scientific and technical conferences:

- 20th International Power Electronics and Motion Control Conference (PEMC) – IEEE 2022, Brașov, Romania, 25–28 September 2022.
- 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-PowerENG) 2023, Tallinn, Estonia, 14–16 June 2023.
- 18th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-PowerENG) 2024, Gdynia, Poland, 24–26 June 2024.
- **19th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-PowerENG) 2025, Antalya, Turkey, 20–22 May 2025.**

3.1.2. Scientific outcomes

The main objective of this research activity within WP3 – Smart Energy Distribution was the development of an advanced ER architecture suitable for hybrid residential microgrids. The proposed system enables the integration of photovoltaic panels, battery storage systems, AC and DC loads, and the utility grid through a unified power conversion structure. By intelligently controlling the power exchange between these subsystems, the ER contributes to improved energy utilization, reduced distribution losses, and enhanced operational flexibility in both grid-connected and islanded modes. The following sections describe the different aspects of the scientific work, covering mentioned above sub-tasks of Task 3.1.

- **Protection and Grounding**

In order to eliminate leakage currents and subsequently improve safety and security, the use of a common-ground inverter in the ER structure was proposed. In many PV-based and hybrid microgrid systems, galvanic isolation is typically employed to mitigate leakage currents and ensure safety. However, the use of isolation transformers significantly increases system size, weight, and cost. It is also shown that even in an isolated case, leakage currents can still pass through in interwinding capacitors and insulation resistance. In case of negative line grounding on the DC side, it can also create dc component in the leakage current. The leakage current can flow between the ac grid and the dc system through the stray capacitor and the insulation resistance of the primary and secondary transformer, as demonstrated in Fig. 1 and Fig. 2.
Fig. 1(a) shows the first condition when the dc microgrid is grounded at a negative point. For this configuration, since the ground on the dc side is at the negative point, a bias voltage proportional to the dc

side voltage will be added to the equivalent circuit. Therefore, in this case, leakage current may have a dc component. Fig. 1(b) shows the equivalent circuit for the leakage current paths in this connection type.
Fig. 2.(a) shows the case where the dc microgrid has middle-point grounding. Fig. 2.(b) shows the simplified equivalent common-mode circuit. Due to the middle-point grounding in the dc side, there will be no bias voltage in the equivalent circuit (bias voltage sources will cancel each other). In this case, there is only a common-mode voltage source, which can lead to high-frequency ac leakage current in this case. Therefore, middle point grounding was recommended in this case to remove dc leakage.

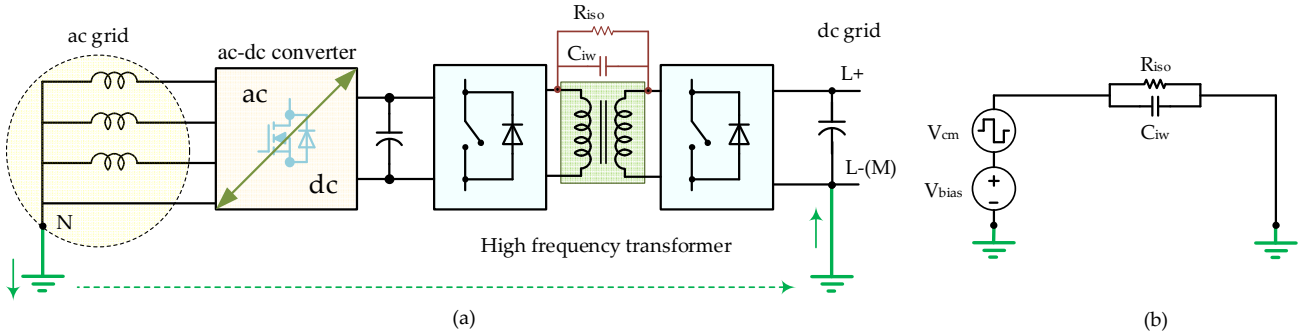


Fig. 1. Leakage current path of high-frequency isolated connection for the unipolar dc system: (a) general circuit; (b) simplified equivalent common-mode circuit.

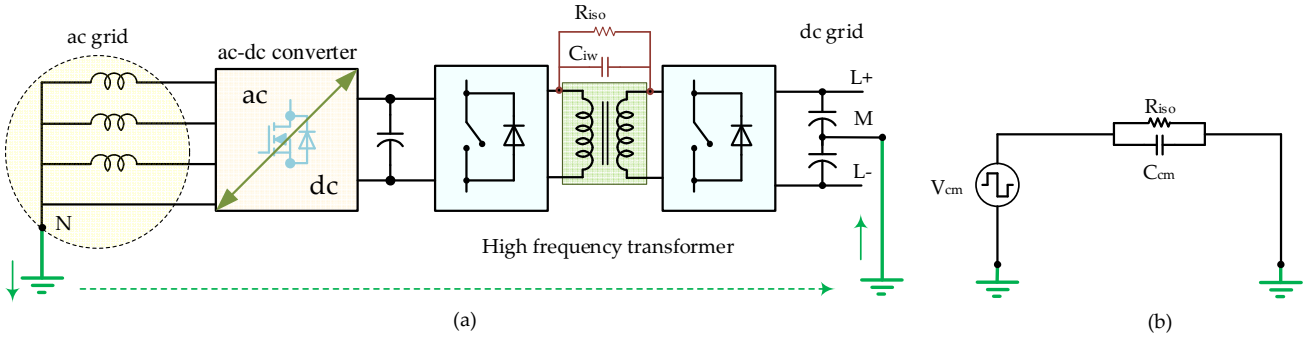


Fig. 2. Leakage current path of high-frequency isolated connection for the bipolar dc system (grounded at the middle point): (a) general circuit; (b) simplified equivalent common-mode circuit.

Therefore, to increase efficiency and reduce the cost, volume, and weight, the non-isolated structures were considered to replace the isolated ones. At the same time, the absence of isolation applies a significant limitation on the grounding possibilities on both sides. Depending on the condition of the switches, a direct electrical path can be created through the grounds on both sides. To solve this, common-ground inverters were used that use the same ground on both sides and eliminate leakage current paths.
It was shown that the best solution for the non-isolated connection of dc microgrids to the ac grids can be the use of common-ground structures. In this case, considering that the negative pole of the dc system and the neutral of the ac grid are directly connected to each other, a similar or even an asymmetrical grounding method can be used for both sides. In the common-ground structure, the common-mode voltage on the dc negative and the ac neutral is clamped to zero and their stray capacitors are bypassed. Therefore, ac leakage current can be eliminated. The dc leakage current can also pass through the insulation resistance, ground on the dc side of the system. To solve this, a TN-S-CD type of connection should be used on the dc side. Fig. 3 shows the general view of this solution.

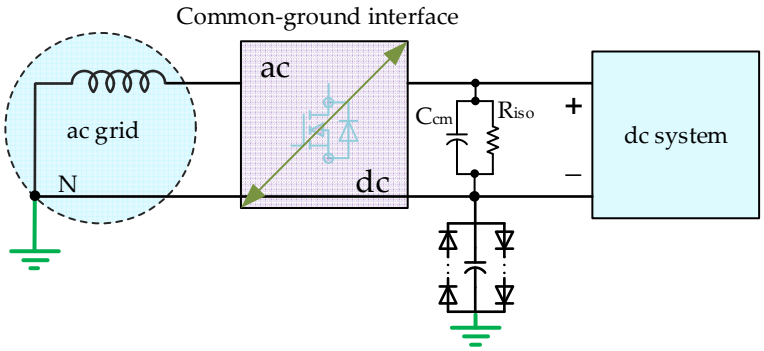


Fig. 3. Common-grounded inverter and elimination of the leakage current path.

As mentioned, common-ground structures are a reliable solution to mitigate leakage currents. At the same time, to protect personnel and equipment, RCD is installed in the grid-side input. The neutral point of ac grid is solidly grounded, which is also connected to the M (L-) point in dc part, eliminating leakage current paths. As can be seen in Fig. 4, bodies of loads, inverter, etc, are connected to the ground through the ground impedance Z_{gDC}. In the case when a person touches the hot line (L+) and the residual current path, the residual current will pass through the capacitors in the inverter structure and the neutral wire of ac side. Therefore, the RCD will trip and disconnect the grid.

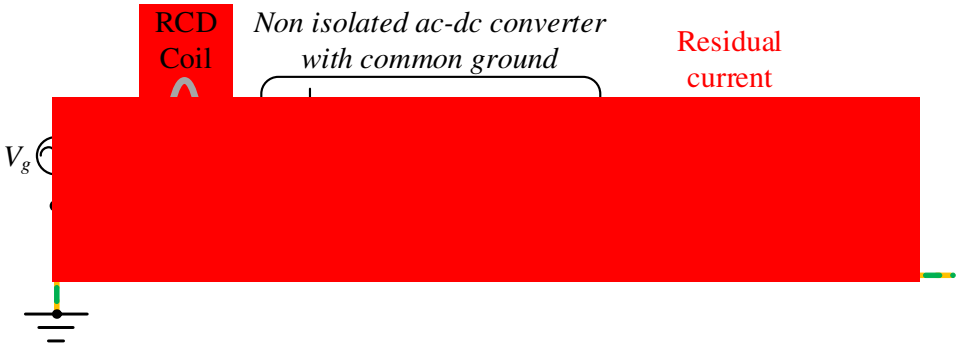


Fig. 4. Protection and grounding for the proposed ER and residual current path in case of touching the hot line.

As the conclusion of the work on this sub-task, it should be mentioned, that **LVdc is increasing and developing in the distribution sector; however, as it was shown in the research, there are still no sufficient standards and studies in the field of dc system protection and grounding. To solve the issue of the improvement of the safety in dc systems, all types of grounding methods in the dc system and at the connection point of the dc to the ac grid were examined. Based on their comprehensive analysis, the dc and the ac leakage current paths were identified, and finally, the advantages and disadvantages of all possible grounding techniques were articulated. Finally, the following conclusions of findings can be highlighted:**

1. Even in the presence of galvanic isolation by means of high-frequency transformer, leakage current can't be eliminated due to the stray inter-winding parasitic capacitance between primary and secondary sides. In case of grounding on ac side (TN or TT configurations), leakage current originated from dc side will be injected into the ac side via mentioned stray capacitance. Low-frequency transformer eliminates this pass completely and can be considered as a solution for leakage current elimination.
2. Even in presence of high-frequency and low-frequency isolation, a dc component in the leakage current can be originated by dc voltage bias between the middle (or negative) point of the dc system and the neutral point of the ac system. In order to eliminate this component, the configurations where there is no voltage bias between the neutral point of the ac system and the middle point of the dc system are recommended.
3. Grounding based on the middle point based on the TN-S-CD type is a highly recommended solution in the dc system grounding. In addition to fault or minimization of electric shock, it eliminates the dc leakage current between the ac and the dc system.

4. Non-isolated common-ground solution for interlinking dc and ac grids can be recommended as an alternative, cost-effective solution where the leakage current between the ac and the dc grid can be completely eliminated.

Provided analysis and conclusions create the foundation for further research with the focus on the analysis of common-ground structures that have higher capabilities, such as a high-power range, higher output quality in bi-directional operation, and can be used at the connection point. In addition, practical solutions to reduce or eliminate the leakage current at the connection point, as well as methods for fault detection according to these grounding configurations, can be further analyzed.

- Proposed Energy Router Architecture

In this work, a single-cell non-isolated multiport ER architecture has been proposed to address the challenges of complexity, cost, and efficiency in conventional microgrid interfaces. Fig. 5 shows the general structure of the proposed ER. The system is built around a central DC-link, which acts as the main energy exchange node connecting different subsystems, including:

- photovoltaic generation units,
- battery storage systems,
- AC loads,
- DC loads,
- and the utility grid.

The non-isolated common-ground inverter was proposed to be used in the ER structure. As a result, as it was mentioned in the above, leakage current paths can be effectively mitigated while eliminating the need for bulky isolation transformers. This approach not only enhances system safety but also contributes to higher power density, reduced system cost, and improved integration capability for residential energy systems.

Furthermore, the architecture incorporates appropriate protection elements, including solid-state circuit breakers (SSCBs), to ensure fast fault isolation and reliable system operation under abnormal conditions.

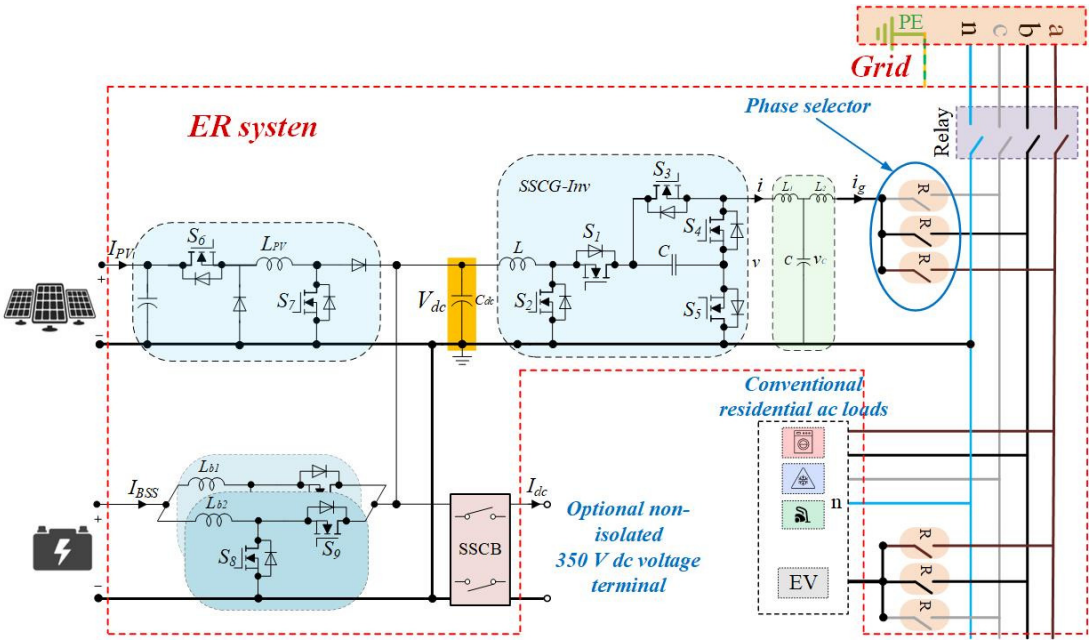


Fig. 5. Concept of proposed SC-TP multiport ER.

Unlike conventional three-phase multi-cell solutions, the proposed architecture of energy router adopts a Single-Cell Three-Phase (SC-TP) topology. This configuration enables the ER to dynamically connect to any of the three phases of the utility grid through a phase-selection mechanism. Such an approach significantly reduces the required number of conversion stages and power electronic components, leading to lower system cost, reduced hardware complexity, and improved overall efficiency.

The proposed SC-TP configuration also contributes to phase balancing in residential distribution networks, where power consumption across phases is often uneven. By enabling dynamic phase selection and

intelligent power routing, the system can support more balanced power distribution and enhance grid stability.

The structure of the single-stage common-ground inverter used in the proposed ER has five switches, a capacitor, and an inductor. For this converter to be able to produce a sinusoidal output from the input DC voltage, it is necessary to have the ability to operate in three different conditions: boost, buck, and buck-boost modes. To have a sinusoidal output voltage curve in the positive half cycle, when the output voltage is lower than the DC voltage, the converter should work in buck mode, and when the output voltage is higher, in boost mode. In the negative half cycle, the situation is completely different. In this case, this structure should work like a buck-boost converter because the polarity of its output voltage is negative.

A central DC bus (highlighted in orange) acts as the system backbone, interconnecting all power sources, inverters, and DC loads. This bus also facilitates potential interconnection with other nanogrids, thereby enhancing system scalability. For load management, AC loads are positioned between the inverter and the grid, enabling seamless operation in both grid-connected and islanded modes. Relays are deployed on the grid, inverter, and load sides to dynamically connect the inverter to the appropriate phase and supply AC loads accordingly. On the source side, both the PV system and BSS are interfaced with the DC bus through dedicated DC-DC converters. The PV converter operates in buck and boost modes, depending on the panel's output voltage, while the BSS is connected via a bidirectional interleaved DC-DC converter that efficiently manages high charging/discharging currents.

Focusing on the common-ground inverter, its modulation was analyzed for different modes to produce a sinusoidal voltage waveform: boost mode, buck mode and buck-boost operation. Corresponding inverter switching patterns for all 5 active switches were also analyzed. Analytical equations, describing the relations between input, output voltages and duty cycles were found and used for the operational analysis. **Besides the component design for different parts, it was shown that using a common-ground inverter not only eliminates leakage current paths but also provides grounding for both sides without isolation and subsequently lowers the weight and cost. It was demonstrated in the work, that RCD will trip in the event of leakage current on both dc and ac sides, ensuring safety. The used DCCB also protected against short circuits with minimum components and reliable operation.**

- **Control Strategy Based on Flatness-Based Control**

Effective control of hybrid microgrid interfaces is crucial to guarantee stable and efficient energy flow among different system components. In the proposed ER, particular attention is given to the regulation of the DC-link voltage, which acts as the central energy coupling point of the entire system.

Due to the strong dynamic interaction between the DC-link and all connected subsystems, including PV generation, battery storage, AC loads, and grid interaction, maintaining a stable DC-link voltage under varying operating conditions is a critical requirement. To address this challenge, a Flatness-Based Control (FBC) strategy has been developed and implemented.

In this work, the FBC approach is applied to the DC-link voltage control loop, enabling rapid stabilization of the DC-link under transient load changes and power fluctuations. For the grid current control loop, a Proportional–Resonant (PR) controller is employed to ensure accurate sinusoidal current tracking and maintain low harmonic distortion in grid-connected operation. The combination of FBC for DC-link regulation and PR control for grid current results in an effective balance between dynamic performance, power quality, and implementation simplicity.

To evaluate the adequate performance of the utilized FBC approach applied to the ER structure, a comprehensive simulation study in the PLECS software was carried out. In the simulation parts, FBC theory is applied to regulate the DC-link voltage in an outer control loop and then the grid current in an inner loop. Under various dynamic conditions, the FBC performance in stabilizing the dc-link and controlling the grid current has been examined and compared with the traditional controller.

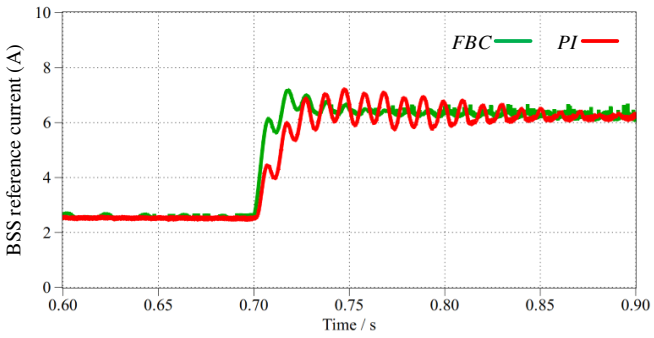
In DC-link control, FBC performance was compared with a PI controller. For the PI controller, the transfer function of the structure for different modes was extracted, and then, using the PID tuner in MATLAB, suitable PI coefficients were chosen. The selected scenario for this evaluation includes step changes in different subsystems in off-grid and grid-connected cases. For instance, a step change in loads or in PV production, a sudden shift in the battery current, or a change mode from charging to discharging mode (or vice versa), or a step change in the direction of the grid-side current to inject or receive power to/from the grid.

1. Dc-link evaluation with FBC (grid-forming)

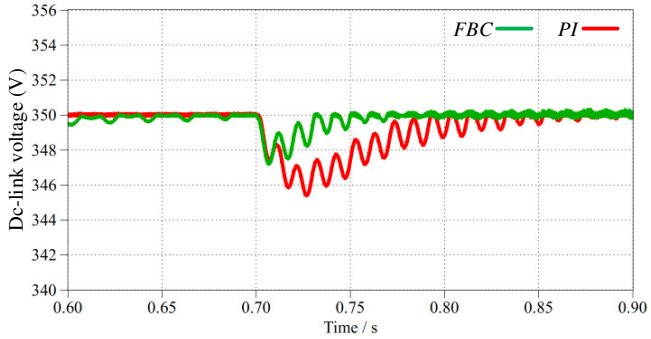
In the grid-forming mode, the BSS regulates the DC-link voltage. The responses obtained with the FBC and PI controllers are shown in Fig. 6. The results indicate that the FBC provides a faster dynamic response and better DC-link voltage regulation. In particular, the DC-link voltage exhibits approximately 3 V undershoot with a settling time of about 50 ms using FBC, whereas the PI controller results in about 5 V undershoot and a settling time close to 150 ms.

2. Dc-link evaluation with FBC (grid-following)

A step change dynamic condition was also applied in the grid-following mode. As shown in Fig. 7, the FBC approach provides a faster response and lower current ripple compared to the PI controller. Consequently, the dc-link voltage remains almost unaffected by the load step when using FBC, whereas with PI control, a noticeable voltage drop occurs and the dc-link requires nearly 1 s to recover to its reference value.

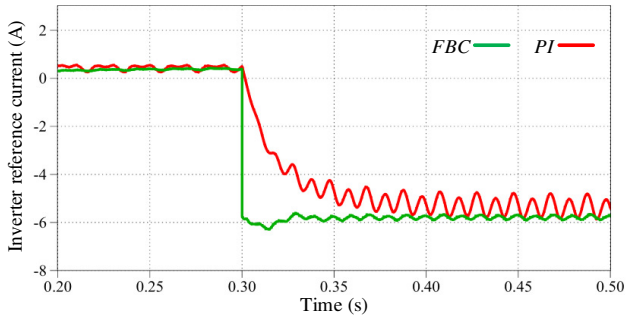


a)



b)

Fig. 6. (a). BSS reference current (control response) for a step change in AC load (grid-forming mode) using FBC and PI, (b). Dc-link voltage and its behavior for the AC load step change.



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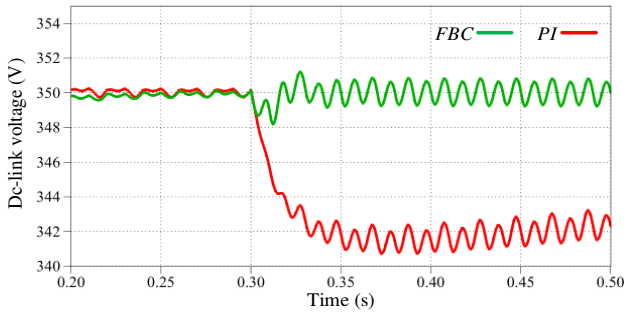
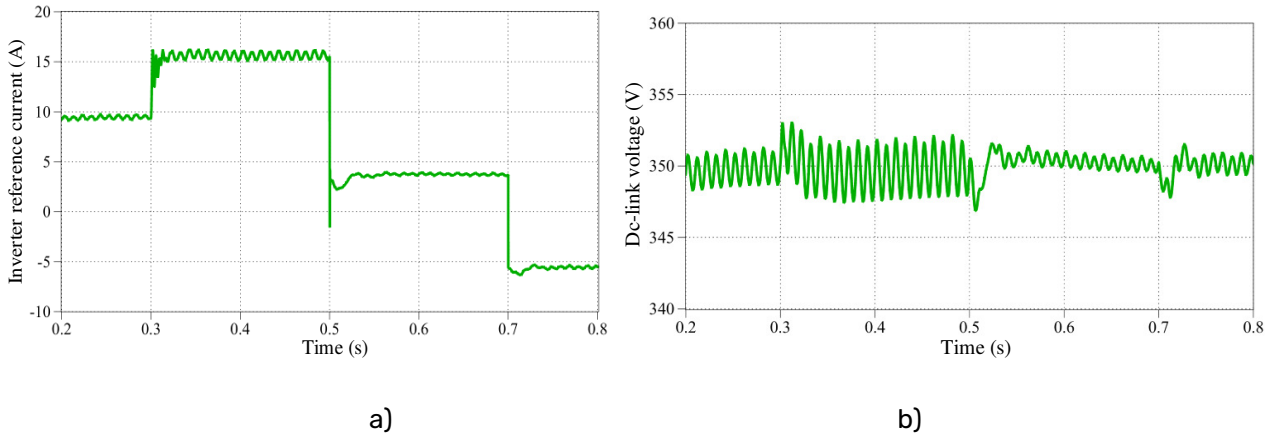


b)

Fig. 7. (a). Inverter reference current (control response) for a step change in DC load using FBC and PI, (b). DC-link voltage and its behavior for DC load step change. In the PI case, it takes almost 1 second to reach its reference.

3. Grid-side evaluation with FBC and PR

To evaluate the performance of FBC in controlling the inverter current injected into the grid, a series of dynamic operating conditions was applied. The results are shown in Fig. 8. The control response, which is the inverter reference current, is shown in Fig. 8 (a), while Fig. 8 (b) shows that the FBC strategy maintains the DC-link voltage close to its reference despite these disturbances and provides fast tracking of the inverter reference current. However, the grid current controlled by FBC exhibits relatively high harmonic distortion as shown in Fig. 8 (c) (about 11.5% THD). To address this issue, a PR controller was employed for the grid-current loop while retaining FBC for DC-link regulation. Although the PR controller shows a slightly slower dynamic response, it significantly improves current quality, reducing the grid-current THD to approximately 3.3% as shown in Fig. 9. Therefore, the combined use of FBC for dc-link control and PR for grid-current regulation was adopted in the experimental implementation.



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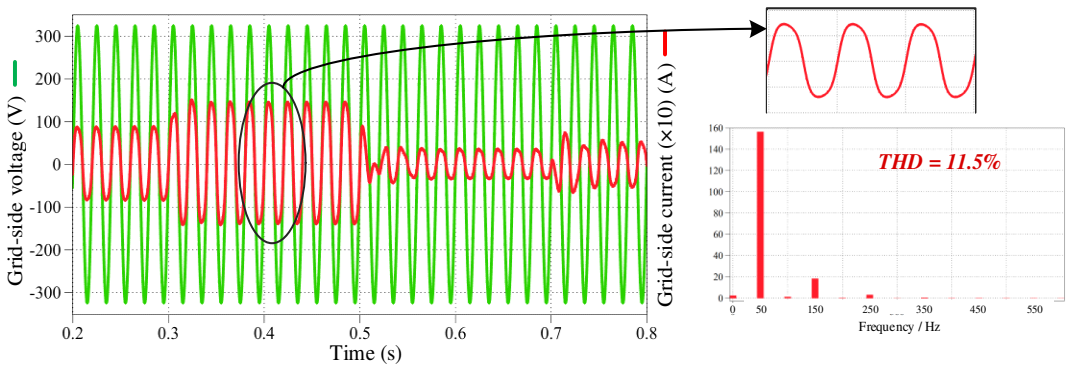


c)

Fig. 8. Results for several different dynamic conditions using FBC (a) Inverter reference current, (b) DC-link voltage, (c) Grid-side voltage and current, along with current frequency spectrum.

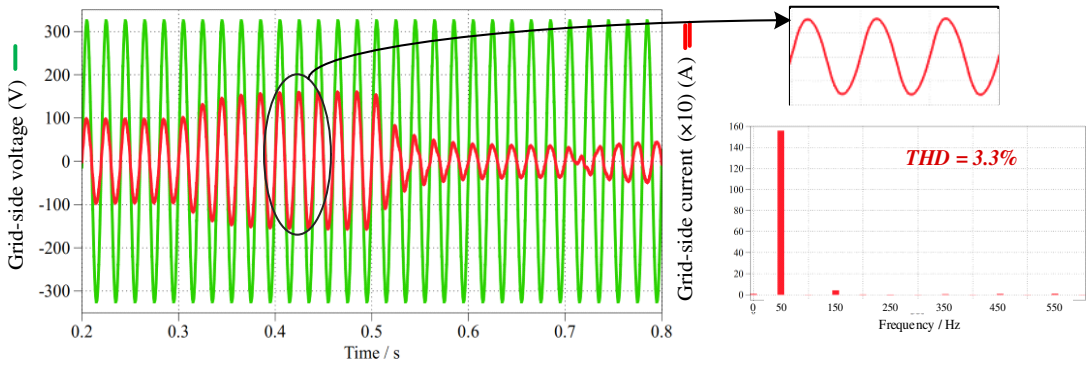


Fig. 9. Grid-side voltage and current (along with current frequency spectrum) under dynamic conditions using PR to control grid current.

The following results and findings were drawn based on a deeply analyzed proposed control system of the energy router in various levels of hierarchy:

1. Two conceptual high-level ER control systems were proposed: a local energy management system and its extension with the edge computing platform and cloud computing platform, providing extended possibilities for energy management.
2. A new flatness-theory-based controller for DC-link voltage regulation in an energy router was proposed, including structure, derivations and design considerations.
3. As grid current controller, it was proposed to use a classical proportional-resonant controller, which ensures fast and robust grid current control.

- **Prototype Development and Experimental Validation**

To validate the feasibility and performance of the proposed ER concept, a laboratory-scale prototype was designed and assembled. The experimental realization of the ER structure and its different parts is illustrated in Fig. 10, while Fig. 11 shows the laboratory setup, including supplies and loads. The processor used in this work is a Texas Instruments TMS320F28379D, and the power switches are SiC-type MOSFETs. ITECH IT6000C bi-directional power supplies are used as a battery and PV emulator. Considering the presence of grid, PV, BSS, and dc/ac loads, experimental tests were conducted under multiple operating scenarios, including:

- DC-mode operation for supplying DC loads,
- grid-forming mode for standalone AC load supply,
- grid-following mode for power exchange with the utility grid,
- and dynamic load change conditions.

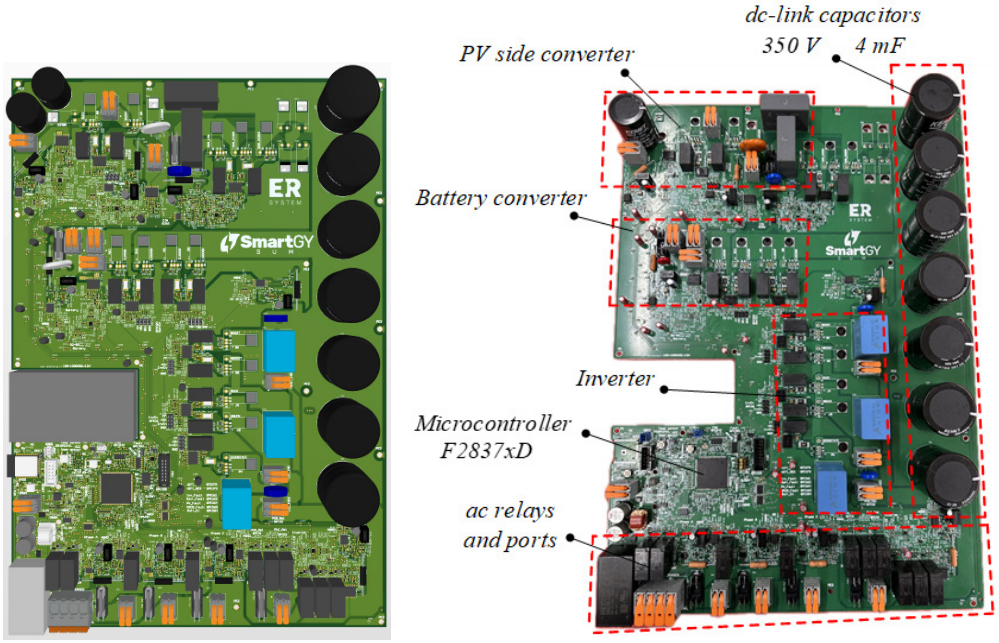


Fig. 10. PCB design and experimental prototype of multiport ER.

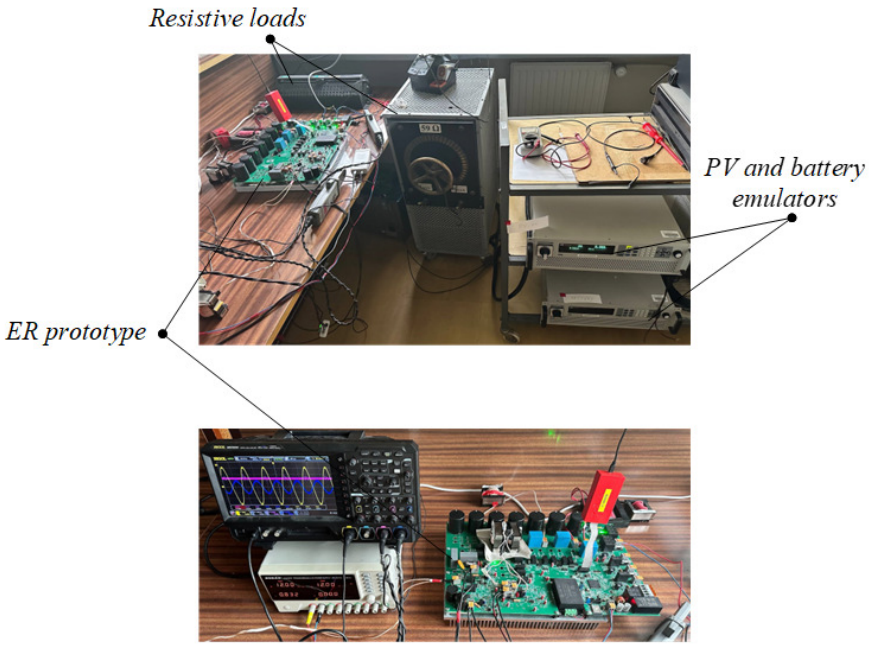


Fig. 11. Laboratory setup.

1. DC Mode

In DC mode, the ER supplies DC loads or connects to other DC nanogrids when grid-forming and grid-following permissions are inactive. This mode is activated once the PV or BSS reaches the operating voltage level. The results in Fig 12 (a) and (b) show that the DC-link voltage is properly regulated while supplying a 194 Ω DC load. When the PV generation exceeds the load demand, the excess power is directed to charge the BSS, indicated by positive PV current and negative BSS current.

2. Grid-Forming Mode

In grid-forming mode, the inverter generates the AC voltage to supply AC loads while maintaining the DC-link voltage. This mode is activated when the PV or BSS reaches the operating level and grid-forming permission is enabled. Experimental results Fig 12 (c) and (d) show that the system can simultaneously supply a 194 Ω DC load and a 59 Ω AC load. The DC-link voltage remains regulated at approximately 350 V, while the AC output voltage is properly generated with the expected double-frequency ripple in the DC-link due to AC power exchange.

3. Grid-Following Mode

In grid-following mode, the system synchronizes with the utility grid and allows bidirectional power exchange. The results demonstrate in Fig 12 (e) and (f) that the energy router can inject power into the grid while maintaining stable DC-link voltage. The grid current is in phase with the grid voltage, indicating unity power factor operation and proper tracking of the reference current.

4. Dynamic conditions

To evaluate control performance under dynamic conditions, a 59 Ω resistive load is connected and disconnected at the ac output while the system continues supplying dc loads. This test is examined in grid-forming mode and it is in the same condition as in the simulation. Fig. 13 (a) and Fig.13(b) present the dc-link voltage alongside the ac voltage and load current. Fig. 5.13(a) captures the moment when a 59 Ω load (830 W) is connected. The controller responds effectively, with minimal dc-link voltage disturbance, approximately 5 V undershoot and a settling time around 40 ms. Fig.13 (c) illustrates the load disconnection, where the controller responds with minimal overshoot and rapid stabilization. Notably, with conventional controllers, such step changes result in significantly slower responses and larger undershoots/overshoots in the dc-link voltage. Fig. 5.13 (c) shows the same dynamic condition using a PI controller. As can be seen in this figure, there is around 35 V undershoot, and the settling time is almost 500 ms. However, by changing PI coefficients, the response might be faster, but undershoot/overshoot will increase, resulting in reaching voltage protection thresholds and subsequently triggering system protection shutdown.

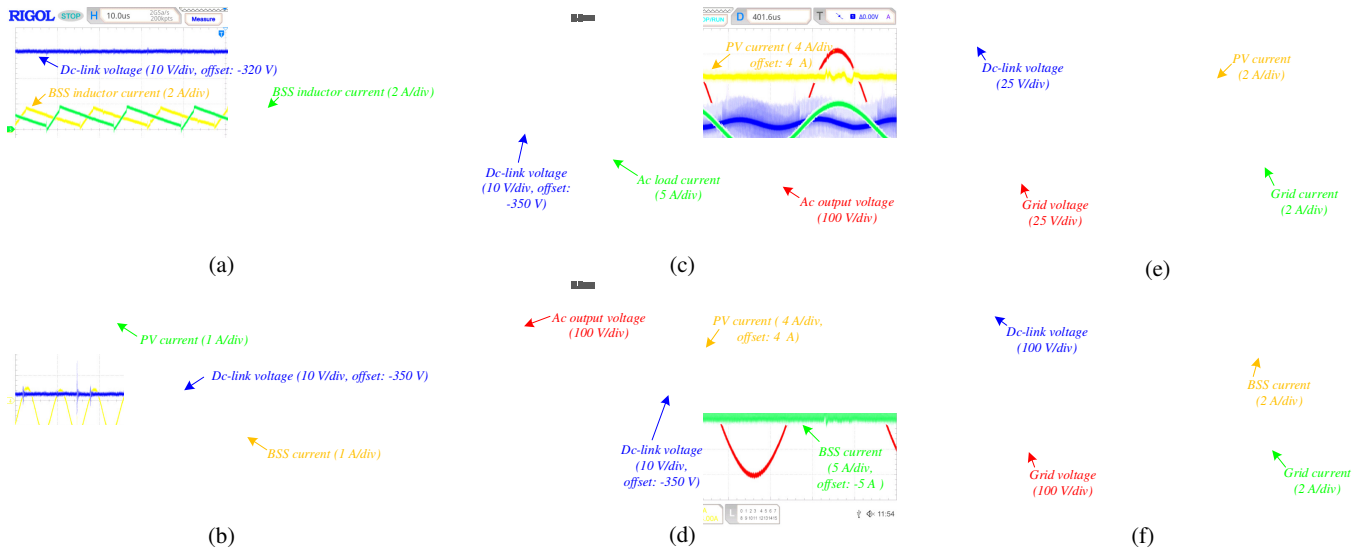
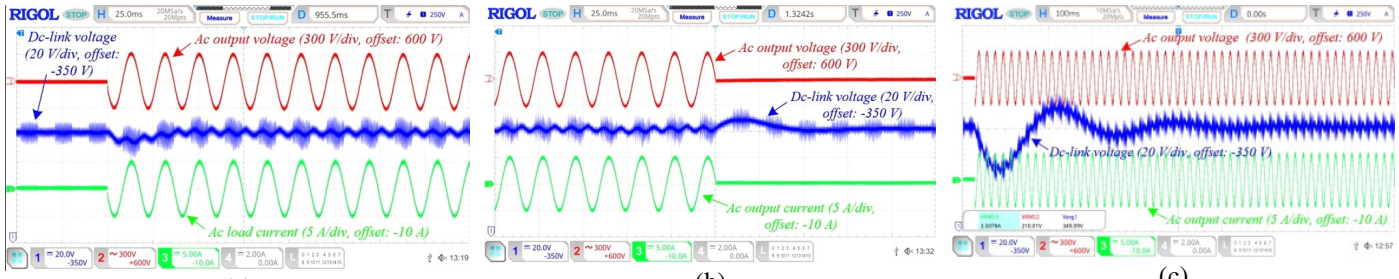


Fig. 12. Experimental results: (a) dc-mode with BSS, (b) dc-mode with PV and BSS, (c) grid-forming with PV, (d) grid-forming with PV and BSS, (e) grid-following with PV, (f) grid-following with BSS.



(a) (b) (c)

Fig. 13. Dc-link voltage under dynamic conditions of (a) adding 830 W (59 Ω) and (b) disconnecting the ac load with FBC, and (c) DC-link voltage under dynamic conditions of adding the same ac load with PI controller.

The following conclusions were obtained in this project:

- 1. While ensuring the required safety and protection, a non-isolated structure was proposed, which offers reduced volume, weight, and cost by eliminating the isolation transformer.
- 2. Although using isolation between the AC grid and the DC nanogrid does not completely suppress leakage currents, the proposed structure based on a common-ground inverter effectively eliminates leakage current paths by establishing a common ground for both AC and DC sides.
- 3. Although the pure DC system in the integration of ZEB to the grid has higher efficiency, due to the current dominance of the AC system, a hybrid structure is a promising solution with relatively high efficiency.
- 4. Considering the growing expansion of DC nano/microgrids, the implementation of appropriate grounding systems is essential to ensure the protection of both personnel and equipment. Unlike previous studies and conventional structures, which often overlook comprehensive protection strategies in the DC link, this study investigated and applied effective grounding techniques. Various connection scenarios were analyzed, and tailored grounding methods were proposed to provide reliable protection on both the AC and DC sides.
- 5. In both high-frequency and low-frequency isolation, a DC component in the leakage current can be created by a DC voltage bias between the middle (or negative) point of the DC system and the neutral point of the AC system. In order to eliminate DC components, special grounding configurations and types were proposed to cancel the voltage bias between the neutral point of the AC system and the middle point of the DC system.
- 6. Unlike conventional architectures that employ a single-cell configuration for single-phase systems and a three-cell design for three-phase systems, the proposed structure adopts a single-cell approach for three-phase operation. This configuration enables dynamic phase selection, contributing to grid balancing and offering considerable economic advantages by reducing hardware complexity and cost.
- 7. In this thesis, the FBC method is employed to enhance dynamic performance. Despite requiring relatively low computational effort, the proposed approach demonstrated notable improvements in dynamic response and significantly enhanced the overall reliability of the system. The FBC solution was used as a promising control method to reach a fast and robust control response.
- 8. For DC-link voltage regulation under dynamic conditions, the FBC demonstrates a much faster and more robust response compared to the conventional PI controller. However, while FBC also provides a fast response in grid current control, the resulting current exhibits higher harmonic content and greater THD compared to the PR method.
- 9. It was demonstrated that for a significant step change in load with FBC, the dc-link undershoot is less than 10 V and the settling time is approximately 40 ms. While with PI, there is a near 35V undershoot and a settling time of near 500 ms.
- **10. The simulation and experimental results validated the effectiveness of both the proposed structure and the control method, confirming their robustness for dynamic operating environments.**

3.1.3. Contribution to the WP objectives

The main results of this work can be summarized as follows:

1. Different types of ER topologies as interlink solutions between DC systems and the AC grid were investigated, and an ER topology based on the SC-TP concept was developed. The proposed approach helps mitigate phase imbalance, offering economic advantages by eliminating the need for two additional conversion cells.

2. A comprehensive study analyzing grounding and leakage currents at the connection point of an isolated DC system to an AC grid was performed. It was first demonstrated that in some specific cases, the isolation itself is not enough for dc leakage current elimination. It is recommended to equalize the potential between the DC middle point and the AC neutral point.

3. For the first time, it is demonstrated that a non-isolated ER based on a common-ground inverter can act as an interlink solution between residential DC and AC grids and can be connected to the residential AC system using special grounding and a classical protection scheme.

4. FBC theory was applied to the ER for the first time to improve control response in dynamic conditions and enhance the reliability level of the multiport ER. While conventional methods have a relatively slow response in dynamic conditions, which may trip the protection system, FBC provides a very fast and robust response in these conditions.

The research outcomes of this task contribute directly to the objectives of WP3 – Smart Energy Distribution, which aims to develop innovative solutions for collaborative energy distribution and advanced operational strategies for microgrids.
First, the proposed ER architecture for hybrid microgrids provides a flexible power electronic interface capable of interconnecting photovoltaic systems, battery storage systems, AC/DC loads, and the utility grid through a unified DC-link. This architecture supports efficient energy exchange between different subsystems and contributes to improved coordination between generation and consumption, which aligns with the WP objective of developing new operational strategies for distributed energy systems.
Second, the introduction of a Single-Cell Three-Phase (SC-TP) topology significantly reduces hardware complexity compared to conventional multi-cell solutions while still enabling interaction with three-phase distribution networks. By enabling selectable phase connection, the system can contribute to improved phase balancing in low-voltage networks, supporting more efficient energy distribution and reduced power losses.
Third, the implementation of an advanced Flatness-Based Control (FBC) strategy for DC-link voltage regulation enhances the dynamic performance of the energy router under varying load and generation conditions. Considering that the DC-link is the central energy exchange point of the system and is affected by dynamic interactions from multiple subsystems, fast and robust control is essential for stable microgrid operation. The proposed control approach contributes to improved energy flow management and reliable system performance.
Finally, the development and experimental validation of a laboratory-scale prototype demonstrate the practical feasibility of the proposed architecture and control strategy. The prototype validation under different operating modes—including DC mode, grid-forming mode, grid-following mode, and dynamic load conditions—provides valuable insights into the operation of energy routers in hybrid microgrid environments.

Overall, the outcomes of this research support the goals of WP3 by contributing to the design of advanced power electronic devices for distribution infrastructures, improving energy flow coordination in microgrids, and enabling more efficient and resilient smart energy distribution systems.

3.1.4. Scientific achievements

Experimental prototypes

#	Name	Description	Status	Photo
1	Energy Router (ER)	ER experimental prototype was designed, assembled and tested during the project. Different tests were conducted to check different operating modes and dynamic conditions.	tested	

Publication

#	Title, incl. citation information	Type	Status	DOI
1	Comparative Evaluation of Isolated dc-dc Converters for Low Power Applications (5 citations)	Conference	Published	10.1109/PEMC51159.2022.9962944
2	Back-to-back energy router based on common-ground inverters (5 citations)	Conference	Published	10.1109/CPE-POWERENG58103.2023.10227480
3	Grounding and isolation requirements in dc microgrids: Overview and critical analysis (12 citations)	journal	Published	10.3390/en16237747
4	Dc Leakage Current in Isolated Grid-Connected dc Nanogrid-Origins and Elimination Methods (2 citations)	Conference	Published	10.1109/CPE-POWERENG60842.2024.10604426
5	Energy Router: A Sustainable Solution for Future Residential Buildings (8 citations)	journal	Published	10.1109/MPEL.2024.3525349
6	Fast and Robust Energy Router Control in Dynamic Conditions Using Flatness-Based Control Theory (0 citations)	Conference	Published	10.1109/CPE-POWERENG63314.2025.11027260
7	Non-Isolated Single-Cell Three-Phase Hybrid Energy Router with Improved Dynamic Behavior	journal	Submitted	-

3.2. Task 3.2 – IRP6 "EV chargers, developing an active bidirectional charger able to provide ancillary services"

3.2.1. Introduction

The scientific work was primarily conducted at the Gdańsk University of Technology (Department of Electrical and Control Engineering) under the supervision of Professor Ryszard Strzelecki. Two additional secondments took place at the University of Extremadura (Department of Electrical, Electronic, and Control Engineering) under the guidance of Professor Enrique Romero-Cadaval.

The first secondment (28.02.2023–29.04.2023) focused on simulations in PLECS and MATLAB of a bidirectional EV charger connected to DC traction grids, evaluation of ancillary services to improve grid quality and efficiency and preparation of a conference paper presenting the results.

The second secondment (22.09.2024–30.11.2024) involved hardware-in-the-loop (HIL) testing of the developed control system for a multi-active bridge converter, development of low- and high-level control algorithms using the TMS320F28379D from Texas Instruments and control system verification using the PLECS RT Box. Additional activities included attendance at the IECON 2024 conference, preparation of a preliminary journal manuscript with HIL results and development of a control board and drivers for the converter prototype.

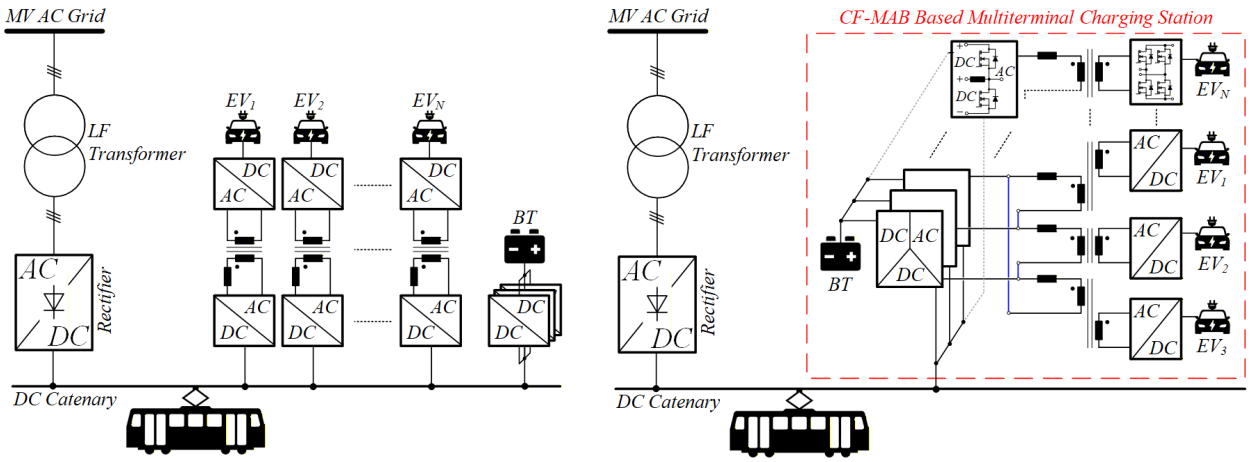
A third secondment took place in Gdańsk, Poland, at the facilities of the project partner MMB Drives Sp. z o.o. (17.02.2025–17.05.2025). The work included development of the prototype's main control, driver and auxiliary boards for a current-fed multi-active bridge converter; implementation and HIL-based validation of the controller software and collaboration with the engineering team to optimize control algorithms and power-flow management.

Work across the participating institutions established strong collaboration and shared scientific outcomes, while the secondment at MMB Drives contributed to the development of a bidirectional EV charger prototype.

3.2.2. Scientific outcomes

1. How CF-MAB converter idea occurred?

Usage of independent converters for each EV (Fig. 1.1a) allows to easily scale number of chargers connected to the DC grid, providing high flexibility and scalability. From the other side, the number of components in the multiterminal charging station, based on such an architecture increases proportionally with a number of EV ports required. For example, installing a multiterminal charging station with N EV chargers based on DAB converters and one BES based on 3-phase interleaved half-bridge converter would require 6N+6 transistors. Number of all other components like transistor drivers, processors, passive components, filters, etc. would also scale proportionally, affecting the final complexity of the system. One of the alternative approaches, which allows to reduce number of required elements in the system, is usage of multiport converters (Fig. 1.1b). Main benefit of multiport DC-DC converters is their higher components utilizations ratio in comparison to conventional connection due to the common sharing of components, which reduces systems price, increases efficiency and makes multiport converters promising solution for the DC grid applications.



a) b)

Figure 1.1. Proposed structure of multiterminal EV charging station with integrated buffer battery, based on a independent converters (a) and studied multiport CF-MAB converter (b).

One of the multiport solutions, widely studied in the literature is the multiple active bridge (MAB) converter, which consists of active bridges connected with a common transformer core, e.g. Triple Active Bridge (TAB) or Quad-Active Bridge (QAB) (Fig. 1.2a). Such connection requires low number of switches, but due to ports dependency on each other, its control is quite complex for a high amount of ports, especially for the multi-terminal EV charging stations application, where each port operates with different power and voltage level. To overcome ports dependency problem, MAB converter with single phase transformers are used (Fig. 1.2b), which allows independent charging of N EVs using a reduced number of switches. However, there is no dedicated port for a BES and the problem of EVs being charged from an unstable DC traction grid, which increases requirements for the converter. To prevent issues caused by EV charging from an unstable DC grid and to avoid voltage mismatches between the EV and the DC grid, CF-DAB converters can be used. The CF-DAB converter is a combination of DAB converter with a boost converter, which adjusts voltage at the auxiliary DC-link capacitor to achieve voltage matching between DC-link and EV port, improving DAB efficiency by reducing transformer RMS current. However, single phase (Fig. 1.2c) and multi-phase CF-DAB (Fig. 1.2d) converters have no scalability potential, having only three ports. This results in a need to install several CF-DAB converters for a multi-terminal charging station, similar to DAB converters, which results in a high number of switches needed.

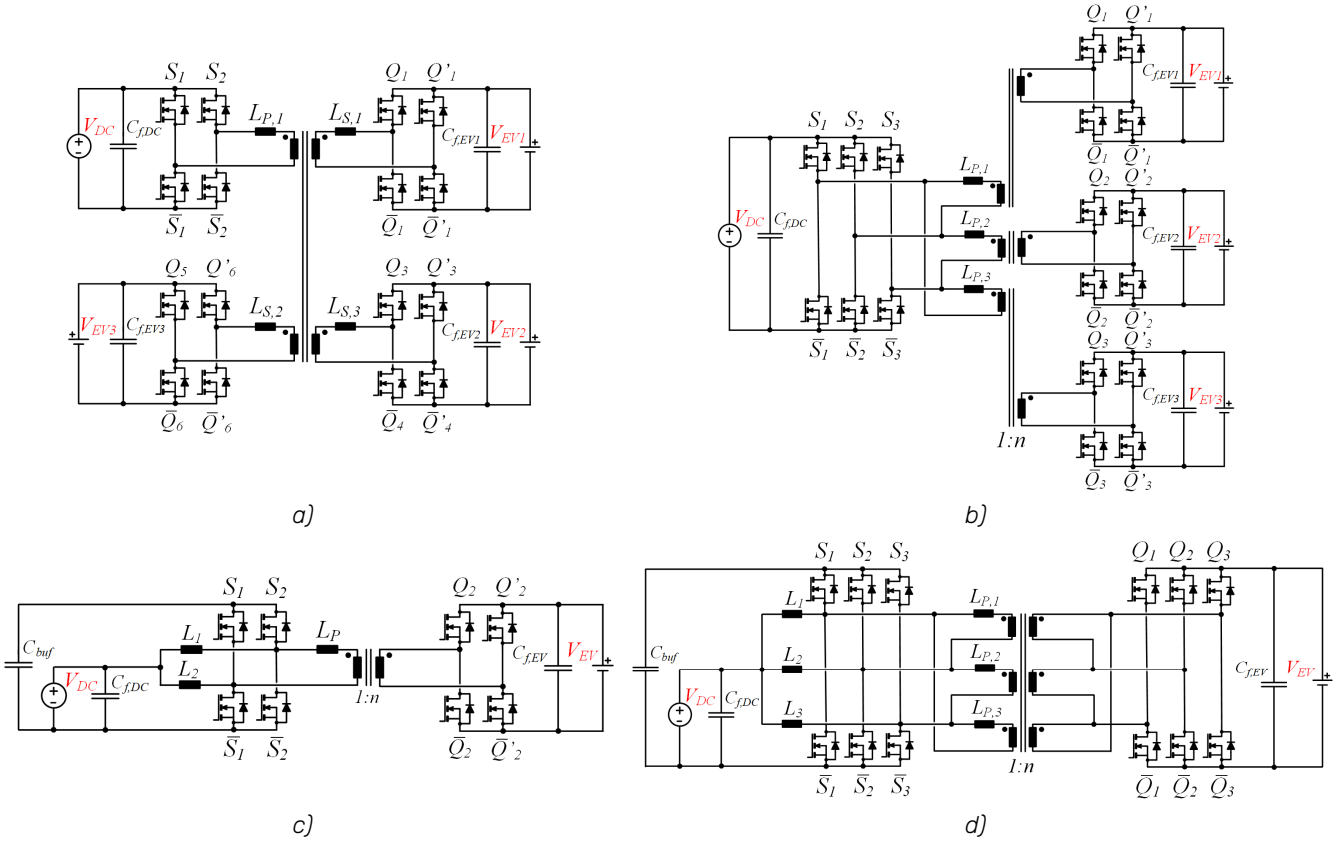


Figure 1.2. Multiport converters suitable for multi-terminal EV charging station: a) Quad-Dual Active Bridge converter with common transformer; b) Multi-Active Bridge converter with single phase transformers; c) Current-Fed Dual Active Bridge (CF-DAB) converter; d) Three-phase CF-DAB converter.

Table 1.1. Multiport converter topologies suitable for multiterminal EV charging station.

Topology	Switches number	Features
Single phase DAB for N EVs + interleaved 3 phase boost for BES	8N+6	-Direct EV charging from unstable DC grid; -Simple ports scaling;
MAB with common transformer	4N+4	-Ports are interdependent; -Complex ports scaling;
MAB with single phase transformers for N EVs + interleaved 3-phase boost for BES	6N+6	-Direct EV charging from unstable DC grid; -Moderate ports scaling;
CF-DAB for each EV and BES	8N	-EV charging from a stable DC-link; -Voltage matching ability;

		-Simple ports scaling;
Studied solution (CF-MAB)	6N	-EV charging from a stable DC port; -Moderate ports scaling;

Alternatively, a combination of a MAB converter with single phase transformers (Fig.1.2c) and a CF-DAB converter (Fig.1.2d) can be used. The proposed in the research converter, referred to as a current-fed Multi-Active Bridge converter (CF-MAB), has a reduced number of switches, allows EV ports scaling, has a dedicated port for BES connection and charges EVs from a stable DC port. Moreover, independent control of power transfer between all ports is possible, which allows flexible converter control and bidirectional EVs operation in a V2G mode. Several solutions that studied CF-MAB converter can be compared to are presented in the literature (Table 1.1).

The main application of the developed converter is particularly relevant, but not limited to multiterminal fast-charging stations located near urban railway transport nodes. The key distinguishing feature of the proposed converter is its scalable structure, which allows, in a cost-effective manner and with minimal additional components, modify the number of ports for EV charging during the development stage, according to demand, needed for a specific multiterminal charging station. Therefore, this research focuses on developing a novel off-board scalable EV fast charger, based on CF-MAB converter topology, capable of providing bidirectional charging.

As were stated previously, the studied CF-MAB converter has one significant benefit in comparison to conventional solutions, which is lower number of transistors required for providing the same functions. However, as will be shown later, the CF-MAB has higher RMS currents and lower transformer utilization ratio, which obviously increases RMS currents of transistors. As a result, further, CF-MAB converter is compared to conventional solutions, based on independent connection of 3-phase interleaved converter for BT charging and three DAB converters for EVs charging. The comparison is done for switches RMS currents and total devices rating.

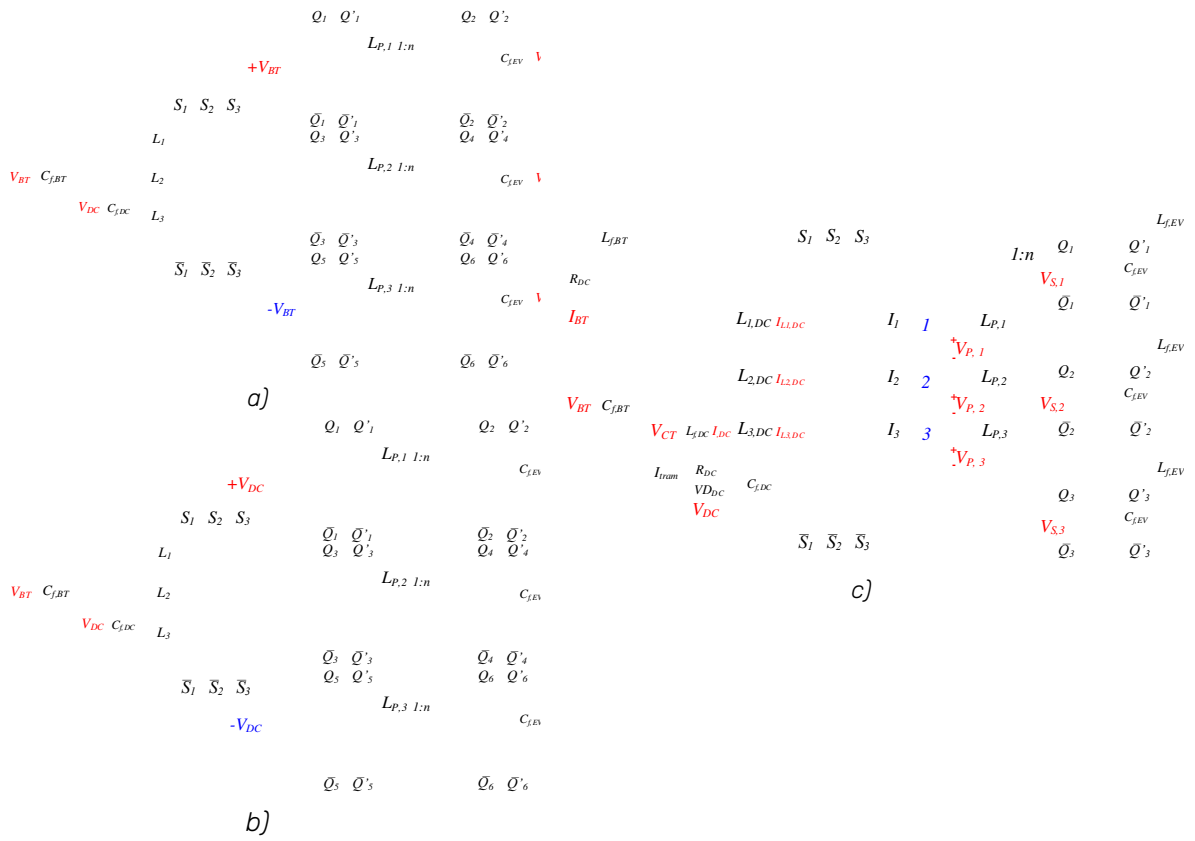


Figure 1.3. Multi-terminal charging station architectures, based on conventional solutions (a, b) and CF-MAB multiport converter (c). Classical connections consist of 3-phase interleaved converter for BT charging and separate three single-phase DAB converters for EVs charging. Connection a) shows structure with series connection, where storage battery BT is charged from unstable traction grid and EVs are charged from the stable battery port with voltage V_{BT}. Connection b), in its turn, shows parallel connection, where both BT and EVs are connected to low voltage traction DC grid V_{DC}.

To account for the differences between architectures, a Total Device Rating (TDR) coefficient is introduced, which considers both the number of switches and their electrical stress (i.e., peak voltage and RMS current):

$$TDR = \sum_{k=1}^{z} V_k ds \cdot I_k rms \tag{1.1}$$

where $V_k ds$ is a k is the maximum drain-source voltage of the k-th transistor, and $I_k rms$ is its RMS current.

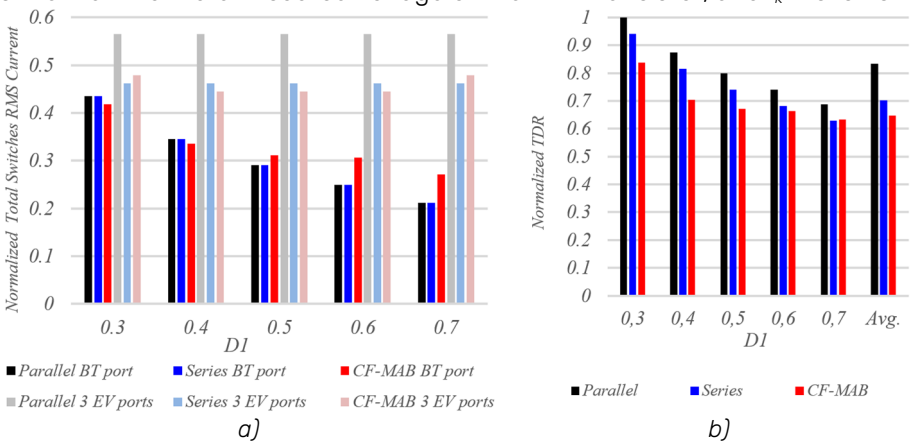


Figure 1.4. Comparison of CF-MAB, parallel and series architectures by normalized total switches RMS currents (a) and total devices rating (b).

The results on Fig. 1.4 show that, in all cases, the CF-MAB converter has lower TDR (10% on average), mostly due to the reduced number of switches. This suggests that the CF-MAB could potentially be less costly than both the series and parallel alternatives.

2. CF-MAB converter operation

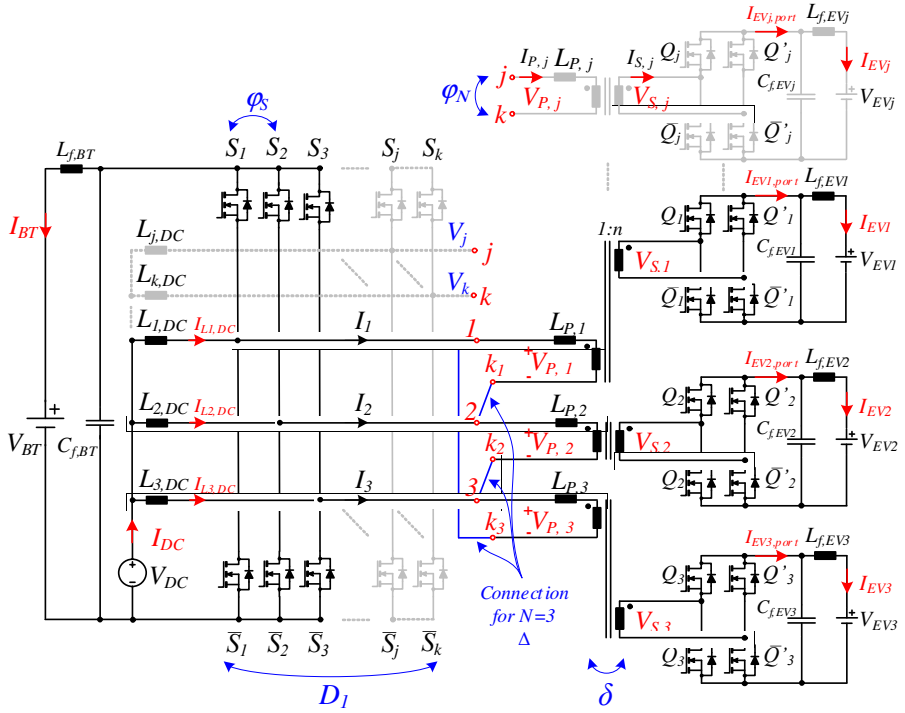


Figure 2.1. Developed during the research CF-MAB converter topology for an arbitrary number of EV charging ports N.

The converter being studied (Fig. 2.1) includes a port for connection to a DC grid, a non-isolated port for battery storage (BT) and N isolated output ports for electric vehicles (EV) charging. On the input side, it uses N interleaved half-bridge stages that operate with phase shifts, similar to an interleaved boost converter. These stages boost the DC grid voltage V_{DC} to match the battery voltage V_{BT} during charging, and step down V_{BT} to match V_{DC} during discharging. As a result, the buffer battery voltage V_{BT} always has to be higher than the DC grid voltage. The high-side primary switches S_1, … , S_N operate with a duty cycle D_1, determined by equation (2.1), while the-low

side switches $\overline{S_1}$, ... , $\overline{S_N}$ operate with a complementary duty cycle $1\text{-}D_1$. The control pulses for the input-side switches S_1, S_2, ..., S_N are phase-shifted by an angle φ_S, which is determined by the number of EV ports and given by $\varphi_S = 2\pi/N$, where number of ports $N=3,5...$

$$D_1 = T_S / T = V_{DC} / V_{BT} \tag{2.1}$$

where $T=T_S+T_{\overline{S}}$, T_S - switch on time.

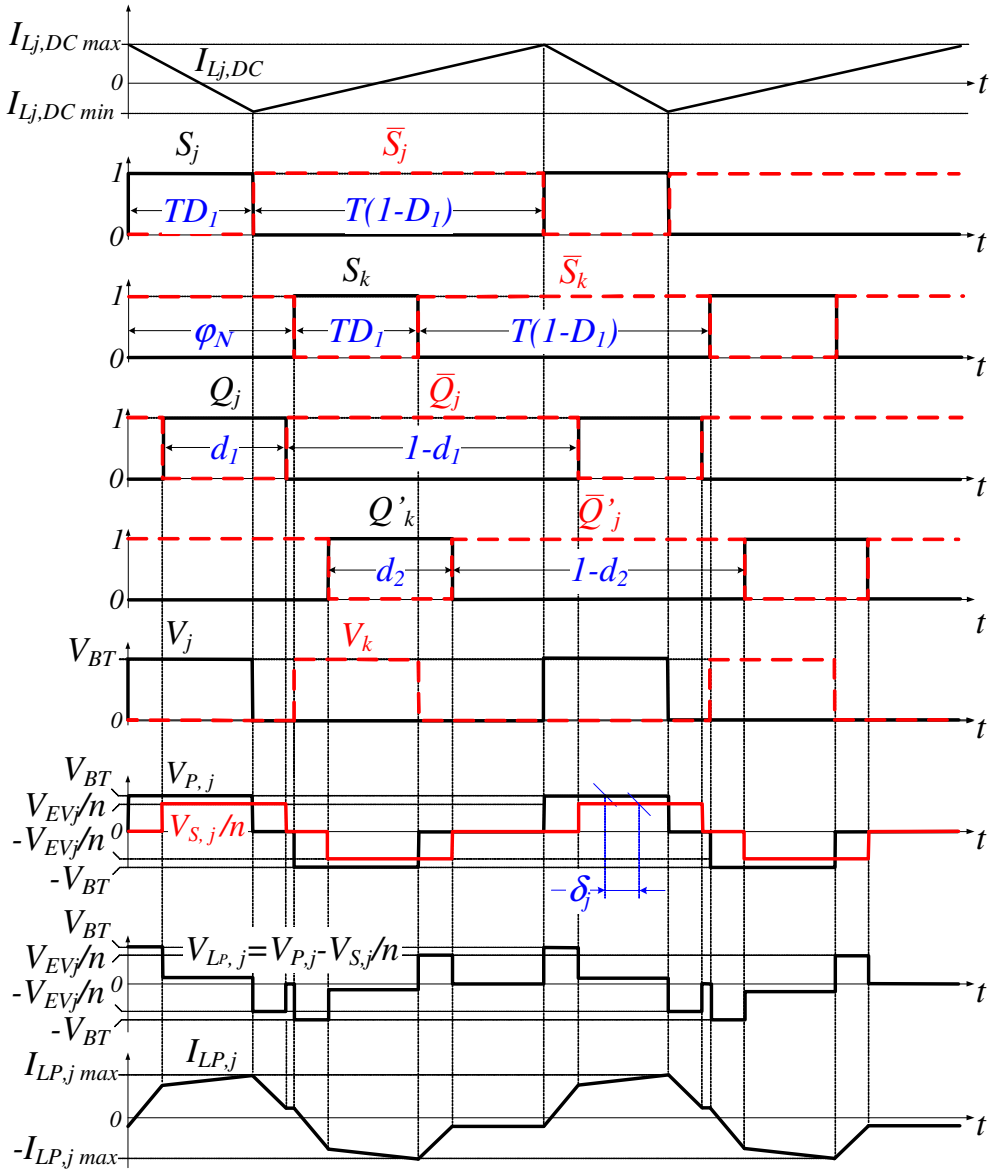


Figure 2.2. CF-MAB converter operating diagrams with SPS modulation.

The EV charging outputs are implemented using N full-bridge AC-DC converters, each electrically isolated from the primary side by a single-phase transformer. The transformer windings are connected to the midpoints of the input-stage half bridges as illustrated Fig. 2.3. The connection points labeled *"j"* and *"k"* correspond to transformer winding terminals, with their indices defined as follows:

$$k = \left(j + (N-1)/2\right) - N \cdot \left\lfloor (2j + N - 1)/2N \right\rfloor \tag{2.2}$$

where $j=1,2, \dots, N$; $\lfloor\ \rfloor$ – floor function.

The phase voltages V_j and V_k, formed between points *"j"* and *"k"* are shifted relative to each other by an angle φ_N. In the simplest case, when $N=3$, the transformer windings are connected in a delta (Δ) configuration, resulting in a phase shifts of $\varphi_S=\varphi_N=120^o$. For the system with more output ports, the phase shift φ_N is calculated using expression $\varphi_N = \pi(N-1)/N$, where $N=3,5,7...$

Output converter side consists of N modules, each of which has Q_j , Q'_j , $\overline{Q_j}$, $\overline{Q'_j}$ switches connected in a full bridge. The Q_j switch operates with a phase shift δ_j regarding the input switch S_j, whereas Q'_j operates with the phase shift δ_j regarding S_k (Fig. 2.2). Control signals between output switches Q_j and Q'_j are phase shifted by an angle φ_N. Both Q_j and Q'_j operate with the same duty cycle D_1. As a result, formed at the secondary side voltage $V_{S,j}$ has the same shape as the input one $V_{P,j}$, but phase shifted by an angle δ_j. Like in a conventional DAB converter, by adjusting the phase shift between primary voltage $V_{P,j}$ and secondary $V_{S,j}$, voltage applied to the leakage inductor $V_{LP,j}$ is changed, which changes current that flows through input and output transformer sides. As a result, by changing δ_j, converter output ports power P_{EVj} is controlled.

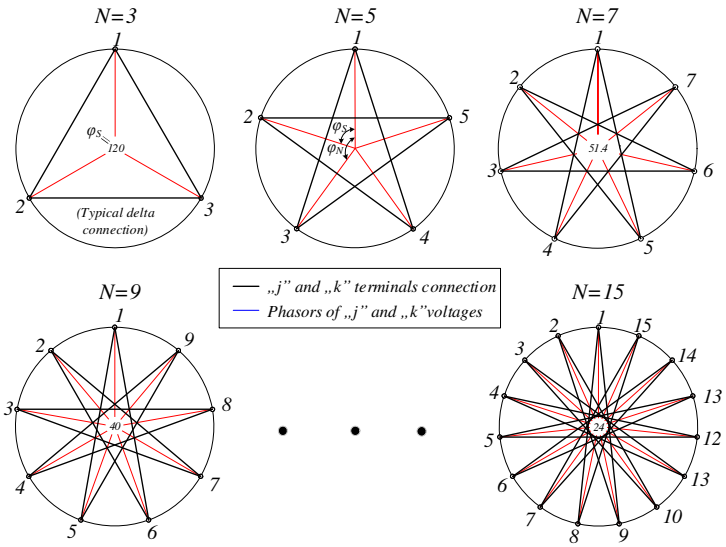


Figure 2.3. Input transformer windings connection diagrams for different number of ports N.

Studied CF-MAB converter operates in several operation areas, which depend on relation between D_1 and δ_j and are presented in the table below.

Table 2.1. Theoretical power characteristics of CF-MAB isolated ports for single phase shift modulation and $|\delta_j| \le \pi/3$.

Phase shift d	*Isolated port power*
$0 \le \lvert\delta_j\rvert \le [\varphi_N - 2\pi D_1]$	$P_1 = \frac{V_{EV,j} V_{BT,j} \cdot \delta_j}{n \cdot 2\pi \cdot f_{sw} \cdot L_{P,j}} \left[2D_1 - \frac{\varphi_N}{2\pi - \varphi_N} \frac{\lvert\delta_j\rvert}{\pi} \right]$
Complementary region: $0 \le \lvert\delta_j\rvert \le [\varphi_N - 2\pi(1-D_1)]$	$P'_1 = \frac{V_{EV,j} V_{BT,j} \cdot \delta_j}{n \cdot 2\pi \cdot f_{sw} \cdot L_{P,j}} \left[2(1-D_1) - \frac{\varphi_N}{2\pi - \varphi_N} \frac{\lvert\delta_j\rvert}{\pi} \right]$
$\lvert\varphi_N - 2\pi D_1\rvert < \lvert\delta_j\rvert < \frac{2\pi}{6}$	$P_2 = \frac{V_{EV,j} V_{BT,j} \delta_j}{8n \cdot \pi^2 \cdot f_{sw} \cdot L_{P,j} \lvert\delta_j\rvert} \left(\left(2\lvert\delta_j\rvert \cdot \varphi_N - \varphi^2{}_N - \frac{4\pi}{2\pi - \varphi_N} \delta_j{}^2 \right) + \left(4D_1 \cdot \varphi_N + 4D_1 \cdot \lvert\delta_j\rvert \right)\pi - 4\pi^2 D_1^2 \right)$
Complementary region: $\lvert\varphi_N - 2\pi(1-D_1)\rvert < \lvert\delta_j\rvert < \frac{2\pi}{6}$	$P'_2 = \frac{V_{EV,j} V_{BT,j} \cdot \delta_j}{8n \cdot \pi^2 \cdot f_{sw} \cdot L_P \cdot \lvert\delta_j\rvert} \left(\left(2\lvert\delta_j\rvert \cdot \varphi_N - \varphi^2{}_N - \frac{4\pi}{2\pi - \varphi_N} \delta_j{}^2 \right) + \left(4\varphi_N (1-D_1) + 4\lvert\delta_j\rvert (1-D_1) \right)\pi - 4\pi^2 (1-D_1)^2 \right)$
$\left(\lvert\delta_j\rvert < 2\pi \cdot (1-D_1) - \varphi_N \right) \cup \left(0 < \lvert\delta_j\rvert < 2\pi D_1 - \varphi_N \right)$	$P_3 = \frac{V_{EV,j} V_{BT,j} \cdot \delta_j}{n \cdot 2\pi \cdot f_{sw} \cdot L_{P,j}} \left(\frac{\varphi_N}{\pi} - \frac{\varphi_N}{2\pi - \varphi_N} \frac{\lvert\delta_j\rvert}{\pi} \right)$

where f_{sw} – keys switching frequency, L_P - transformer leakage inductance, $n=N_2/N_1$ - transformation ratio (N_2-transformer output turns, N_1-input turns).

Equations in the Table 2.1 define converter theoretical regulation characteristics for the phase shift $|\delta_j| \le \pi/3$. As can be seen, different equations are used for different ratios of D_1 and δ_j due to the fact, that voltage across

leakage inductor changes for different phase shift and duty cycle values, which is shown in the Fig. 2.4a. Overall, for single phase shift modulation, there are three basic converter operation regions can be distinguished - P_1, P_2, P_3, whereas P'_1 and P'_2 are complementary and obey the similar relations as P_1 and P_2, but with $1-D_1$. This means, that operation regions are symmetrical with respect to $D_1=0.5$ (Fig. 2.4b).

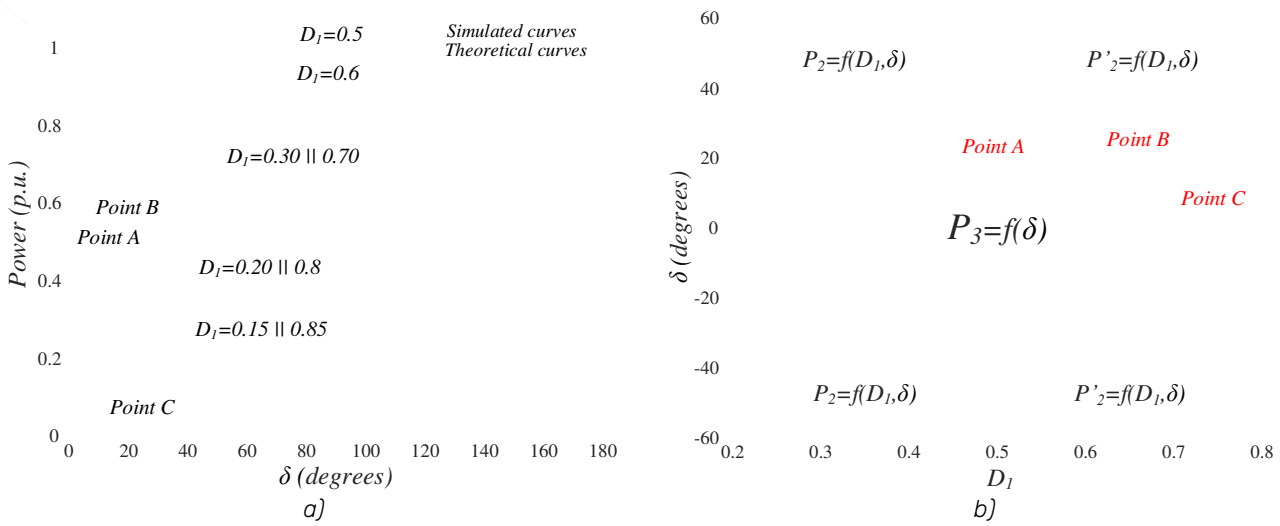


Figure 2.4. CF-MAB theoretical and simulated regulation curves (a) and operation regions for different duty cycle D_1, phase shift δ_j and 3 isolated ports $N=3$. Results are presented for single phase shift modulation.

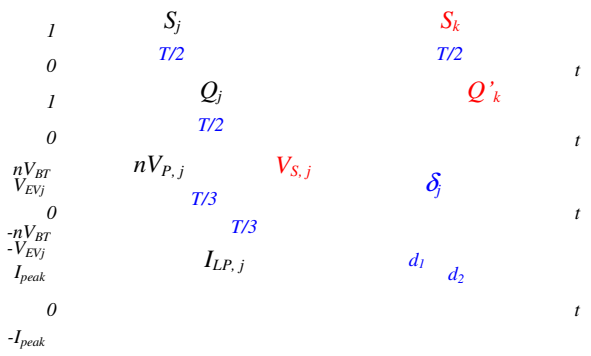
Point A:

$D_1=1/2$

$\delta_j=30^o$

$d_1 = d_2 = T/3$ or $2\pi/3$

Peak power deliver capability over the wide range of phase shift $|\delta_j|$



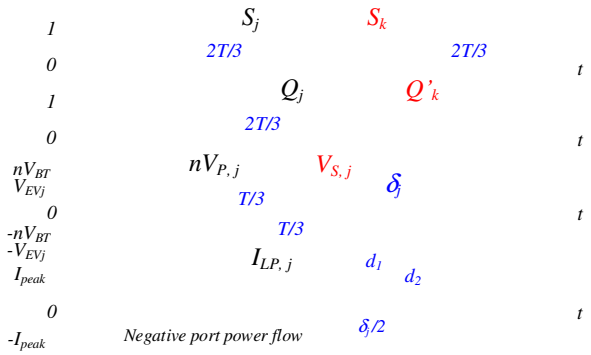
Point B:

$D_1=2/3$

$\delta_j=35^o$

$d_1 = d_2 = T/3$ or $2\pi/3$

Boundary point. Further increase of D_1 would cause d_1 and d_2 decrease. Power deliver capability is slightly lowered due to negative power flow over some time.



Point C:

$D_1=4/5$

$\delta_j=15^o$

$d_1 = d_2 = T(1-D_1) = T/5$ or $2\pi/5$

Power delivery capability is significantly reduced due to low d_1 and d_2

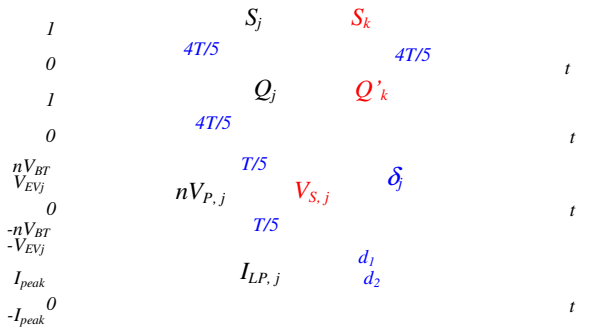


Figure 2.5. Example of one isolated port operation in different points.

In order to verify correctness of the theoretically obtained equations from Table 2.1, modeling of the converter for $N=3$ were made. As can be seen (Fig. 2.4), theoretical and simulated CF-MAB regulation characteristics coincide, which confirms the correctness of the earlier obtained expressions. Since the converter works symmetrically with respect to $D_1=0.5$, the regulation characteristics for D_1 and $(1-D_1)$ are the same. The peak transmitted power of the CF-MAB decreases with a decrease of D_1 and additionally shifts towards smaller values of δ_j. It should be noted that for $D_1=0.5$, the peak in the regulation characteristic occurs at a phase shift of 90°, which is the same as for a single-phase DAB converter characteristic.

An important feature that distinguishes the P_3 from other regions, is the independence of the transmitted power from D_1 (Table 2.1). In all other regions, power of the isolated ports depends on D_1, which means phase shift δ_j has to be regulated to keep EVs charging power constant during significant V_{DC} voltage fluctuations and V_{DC}/V_{BT} mismatches. Independence of the power from D_1 in case of P_3 explained by the fact, that in range of $1/3<D_1<2/3$, duration of positive and negative voltage levels $V_{P,j}$ and $V_{S,j}$ equals to $2\pi/3$ and do not change. Pulses only shift left or right, which can be observed at Fig. 2.5, Point A and Point B. However, even though in both cases $d_1=d_2=2\pi/3$ and current waveforms are similar, in case of Point B, during time $\delta_j/2$, transformer current is negative, while the $V_{S,j}$ is positive. That means power flows from the EV port capacitor back to the input, reducing total power, delivered to the port. That explains dependence of the port power on D_1 even when d_1 and d_2 are constant.

Point C presents a case of a significant mismatch between V_{BT} and V_{DC}, which occurs when $D_1>2/3$. As can be seen from Fig. 2.5 in such case, for the $2(\pi-d_1)$ time during the period, both primary and secondary side voltages are equal to zero, which significantly limits port power (Fig. 2.4a). From the other side, it reduced transformer utilization ratio, because most of the time, there is no power flow through it. Even significant increase of δ_j does not help to reach same power level as can be reached by operating in region P_3. One possible solution might be using a lower value of leakage inductor $L_{P,j}$, to reach desired power level even when $D_1>>2/3$ or $D_1<<1/3$. However, this would increase RMS currents in other regions of operation. Thus, in case of significant V_{DC}/V_{BT} mismatches, it is better to limit power, delivered to the EV port. Especially, considering that such severe voltage mismatches are not common to happen and can be eliminated by proper buffer battery operation.

As a result, considering that most often DAB converters work in the range of $|\delta_j| < \pi/6$ (due to increase in circulating currents when δ_j increases), value of the leakage inductor for $N=3$ and $\varphi_N=2\pi/3$ can be calculated using P_3 equation from the Table 2.1, where $P_{EV(max)}$ is the peak desired power of the port, achieved for the phase shift $|\delta_j|=\pi/6$:

$$L_{P,j(CF-MAB)} \le \frac{V_{EV,j(\min)} V_{BT,j(\min)}}{2n\cdot\pi\cdot f_{sw}\cdot P_{EV(\max)}}\delta_j\left(\frac{\varphi_N}{\pi}-\frac{\varphi_N}{2\pi-\varphi_N}\frac{|\delta_j|}{\pi}\right)\rightarrow L_{P,j(CF-MAB)} \le \frac{V_{EV,j(\min)} V_{BT,j(\min)}}{2n\cdot f_{sw}\cdot P_{EV(\max)}}\frac{7}{72} \quad (2.3)$$

This equation can be compared to the conventional DAB equation, which has the following look for a $\delta=\pi/6$:

$$L_{P(DAB)} \le \frac{V_{EV(\max)} V_{BT(\max)}}{2n\cdot\pi\cdot f_{sw}\cdot P_{EV(\max)}}\delta\left(1-\frac{|\delta|}{\pi}\right)\Bigg|_{\delta=\pi/6}\rightarrow L_{P,j(DAB)} \le \frac{V_{EV(\max)} V_{BT(\max)}}{2n\cdot f_{sw}\cdot P_{EV(\max)}}\frac{10}{72} \quad (2.4)$$

Comparing equation 2.3 to 2.4 it can be seen, that to achieve same power of $P_{EV(max)}$, leakage inductance of the CF-MAB converter port has to be 30% lower in comparison to conventional DAB converter. This means higher peak and RMS transformer currents of the CF-MAB converter in comparison to DAB. From the other side, the difference in the equations can be interpreted as follows: for the same value of leakage inductance $L_{P,j(CF-MAB)}=L_{P(DAB)}$, the power delivered to the output of the CF-MAB isolated port is 30% lower than that of a conventional DAB converter, when all other parameters are the same. The difference, however, decreases for the higher number of isolated ports N, due to increase of $\varphi_N=\pi(N-1)/N$. Thus, for $N\rightarrow\infty$, $\varphi_N=\pi$, and equation 2.3 takes the same form as 2.4.

3. SPS modulation vs mDPS modulation.

During converter operation with a SPS modulation, described earlier, voltages at the primary side of the transformer $V_{P,j}$ and secondary side $V_{S,j}$ have the same form ($d_{P,j}=d_{S,j}$), but phase shifted regarding each other on an angle δ_j. When battery voltage nV_{BT} and EV voltage V_{EVj} are perfectly matched ($nV_{BT}=V_{EVj}$, n – transformation ratio), SPS results in a current waveforms similar to the one on a Fig. 2.5, where during zero voltage intervals, current also equals zero. However, for the studied converter application, voltage of the EV batteries and buffer battery BT changes during charging, causing a voltage mismatch ($nV_{BT}\cdot d_{P,j}\neq V_{EVj}\cdot d_{S,j}$), which leads to a volt-second unbalance across the inductor $L_{P,j}$ and increased RMS current in a transformer. In order to reduce transformer RMS currents, several well-known control methods are used for a single-phase DAB converter, most

advanced of which is a triple phase shift (TPS) modulation. In a TPS modulation, not only phase shift between primary and secondary side voltages δ changes, but also phase shifts between primary δ_P and secondary side half-bridges δ_S (Fig. 3.1b), while switches operate with the duty cycle equal to half of the period $D_1=1/2$. This allows to adjust both primary side d_P and secondary side d_S ($d_P=T/2-\delta_P$, $d_S=T/2-\delta_S$). However, in the studied CF-MAB converter, input side parameters cannot be adjusted to achieve TPS, as change of φ_N would cause loss of interleaving between input side phases, whereas D_1 adjustment would cause change of storage battery current I_{BT}. Thus, only methods that involve secondary side control can be used, like PWM plus phase shift (PPS) and DPS modulation. Despite PPS ability to reduce transformer RMS current, it leads to increased converter switching losses due to additional transistors commutations. Thus, DPS modulation seems to be a better way of matching primary and secondary side voltages for the studied application. However, conventional DPS modulation implies that both input and output side half-bridges operate with a $D_1=1/2$ duty cycle and the phase shift between secondary side bridges δ_S changes in order to adjust d_S (Fig. 3.1a). This works perfectly for the classical DAB converter, where primary and secondary side voltage waveform functions have even symmetry regarding y-axis. However, for the CF-MAB ports, this is true only for one point of $D_1=1/2$, which can be seen on Fig. 2.5 Point A. In all other cases, voltage waveforms are odd functions, which means adjusting only phase shift between secondary side half-bridges is not enough and classical DPS modulation is not applicable for the studied CF-MAB converter. Therefore, a modified version of DPS modulation is described on Fig. 3.2 (with switches duty cycles not equal to 1/2), which allows adjusting output side $d_{S,j}$ to achieve transformer volt-second balance, ensuring $nV_{BT} \cdot d_{P,j} = V_{EV} \cdot d_{S,j}$, and controlling δ_j to achieve required EV port power $P_{EV\,N}$.

Important to note, that due to the fact that maximum $d_{P,j}$ value for the CF-MAB converter with three isolated ports is $d_{P,j}=2\pi/3$, in the whole converter operating range $d_{S,j}$ can be either increased or decreased, which allows matching both $G_j \le 1$ and $G_j > 1$, where coefficient G_j represents voltage mismatch ratio between battery V_{BT} and V_{EV} connected to the port:

$$G_j = \frac{nV_{BT}}{V_{EVj}} \tag{3.1}$$

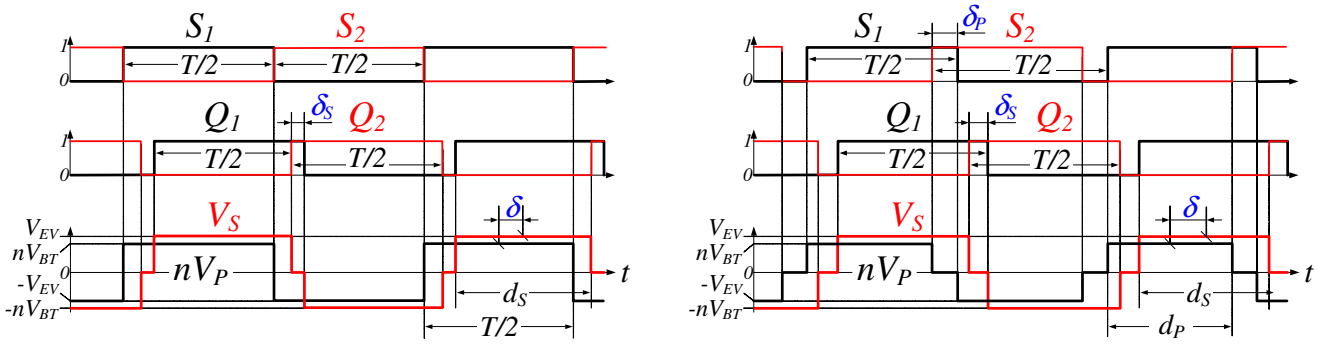


Fig. 3.1. DPS (a) and TPS (b) modulation techniques comparison for conventional single-phase DAB converter.

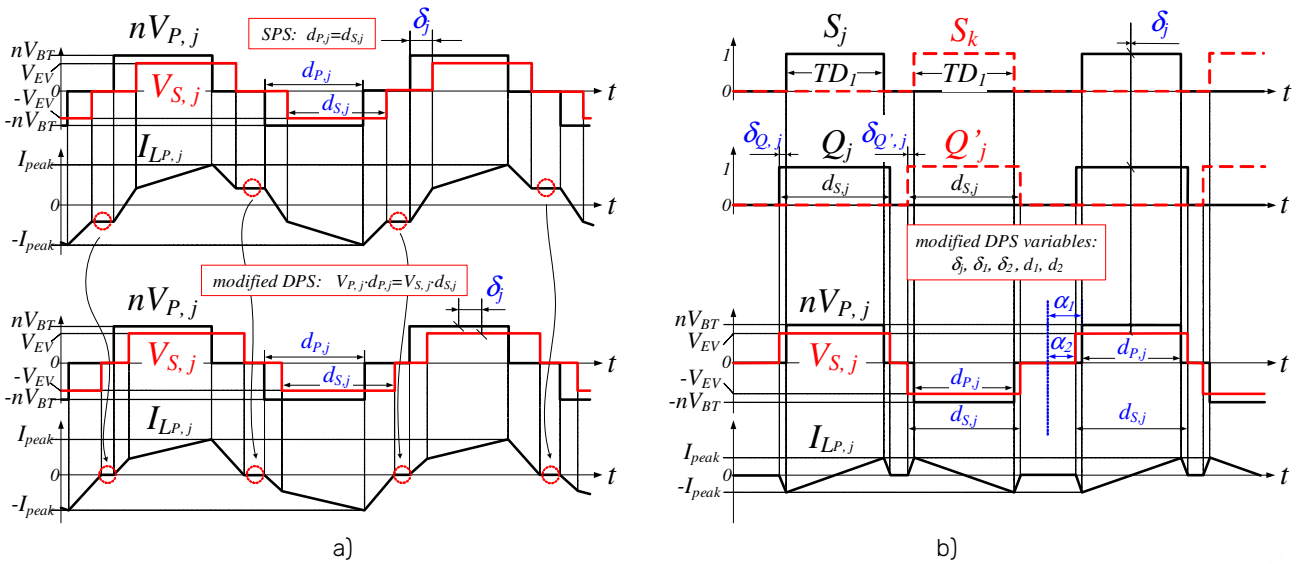


Fig. 3.2. SPS and mDPS modulation techniques comparison for one CF-MAB converter port with V_{BT} and V_{EVj} voltage mismatch. Variables Δ_1 and Δ_2 are not used in a practical application, but used for a theoretical RMS currents calculation.

In order to achieve mDPS modulation, two additional phase shifts $\delta_{Q,j}$ and $\delta_{Q',j}$ for the secondary side switches are introduced, which represent shifts of control pulses for output side transistors Q_j and Q'_j regarding input side transistors S_j and S_k (Fig. 3.2b). The control variables for the mDPS modulation depend on D_1 as well as G_j and are presented in the Table 3.1. There are eight modes of operation for the CF-MAB converter with mDPS modulation can be distinguished, with each mode having different modulation variables $d_{Q,j}$, $d_{Q',j}$, $d_{P,j}$ and $d_{S,j}$. Due to converter symmetrical operation regarding $D_1=0.5$ point, modes 1, 2, 3 and 4 are complementary to 7, 8, 5 and 6 accordingly, which is clearly visible on the Fig. 3.3. Thus, only four of the modes are shown as example in Figure 3.4.

Table 3.1. Calculation of a mDPS modulation variables for different converter operation modes and N=3 ($T=2\pi$).

Regions	Modes	d_1, d_2	δ_1, δ_2
1: $D_1 < \frac{1}{3}$	**1:** $D_1 \cdot G_j < \frac{1}{3}$	$d_{P,j} = TD_1$ $d_{S,j} = TD_1 \cdot G_j$	$\delta_{Q,j} = \delta_{Q',j} = \frac{1}{2}\left(d_{P,j} - d_{S,j}\right)$
	2: $D_1 \cdot G_j \geq \frac{1}{3}$	$d_{P,j} = TD_1$ $d_{S,j} = T\sqrt{\frac{D_1}{3} \cdot G_j}$	$\delta_{Q,j} = \frac{d_{P,j}}{2} - \frac{T}{6}$ $\delta_{Q',j} = \frac{d_{P,j}}{2} + \frac{T}{6} - d_{S,j}$
2: $\frac{1}{3} \leq D_1 < \frac{1}{2}$	**3:** $\frac{G_j}{3D_1} < 1$	$d_{P,j} = \frac{T}{3}$ $d_{S,j} = \frac{T}{3} \cdot G_j$	$\delta_{Q,j} = TD_1 - \frac{T}{3} + \frac{d_{P,j}}{2} - \frac{d_{S,j}}{2}$ $\delta_{Q',j} = \frac{1}{2}\left(d_{P,j} - d_{S,j}\right)$
	4: $\frac{G_j}{3D_1} \geq 1$	$d_{P,j} = \frac{T}{3}$ $d_{S,j} = T\sqrt{\frac{D_1}{3} \cdot G_j}$	$\delta_{Q,j} = \frac{TD_1}{2} - \frac{T}{6}$ $\delta_{Q',j} = \frac{TD_1}{2} + \frac{T}{6} - d_{S,j}$
3: $\frac{1}{2} \leq D_1 \leq \frac{2}{3}$	**5:** $\frac{G_j}{3(1-D_1)} < 1$	$d_{P,j} = \frac{T}{3}$ $d_{S,j} = \frac{T}{3} \cdot G_j$	$\delta_{Q,j} = TD_1 - \frac{T}{6} - \frac{d_{S,j}}{2}$ $\delta_{Q',j} = \frac{T}{6} - \frac{d_{S,j}}{2}$
	6: $\frac{G_j}{3(1-D_1)} \geq 1$	$d_{P,j} = \frac{T}{3}$ $d_{S,j} = T\sqrt{\frac{(1-D_1)}{3} \cdot G_j}$	$\delta_{Q,j} = \frac{TD_1}{2} + \frac{T}{3} - d_{S,j}$ $\delta_{Q',j} = \frac{TD_1}{2} - \frac{T}{3}$
4: $D_1 > \frac{2}{3}$	**7:** $(1-D_1)G_j < \frac{1}{3}$	$d_{P,j} = T(1-D_1)$ $d_{S,j} = T(1-D_1) \cdot G_j$	$\delta_{Q,j} = \frac{TD_1}{2} + \frac{T}{6} - \frac{d_{S,j}}{2}$ $\delta_{Q',j} = \frac{TD_1}{2} - \frac{T}{6} - \frac{d_{S,j}}{2}$
	8: $(1-D_1)G_j \geq \frac{1}{3}$	$d_{P,j} = T(1-D_1)$ $d_{S,j} = T\sqrt{\frac{(1-D_1)}{3} \cdot G_j}$	$\delta_{Q,j} = \frac{TD_1}{2} + \frac{T}{3} - d_{S,j}$ $\delta_{Q',j} = \frac{TD_1}{2} - \frac{T}{3}$

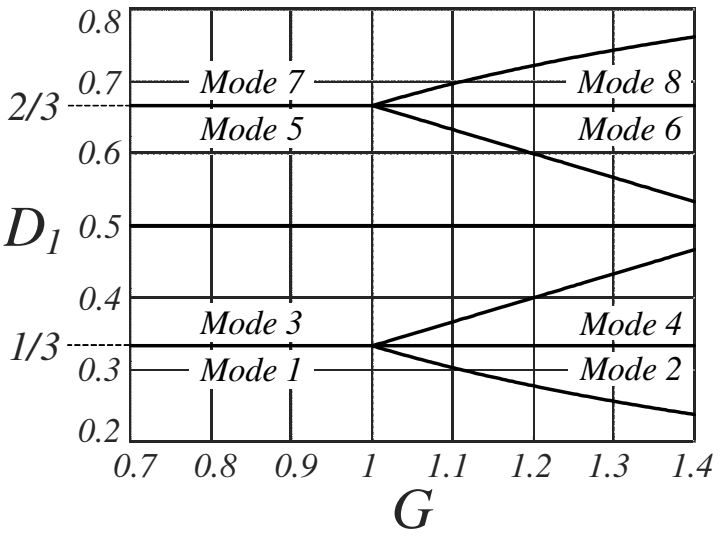
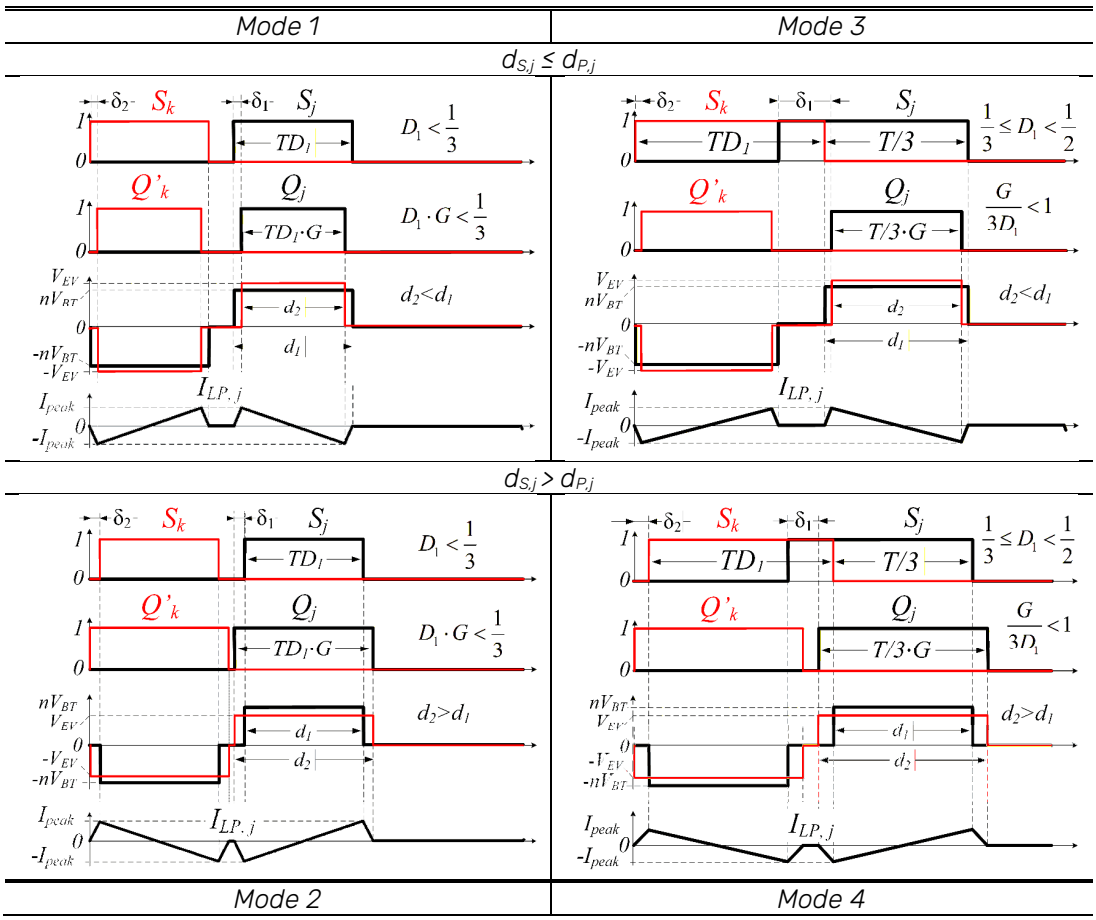


Figure 3.3. Graphical representation of 8 operation modes of the CF-MAB converter, operating with mDPS modulation.



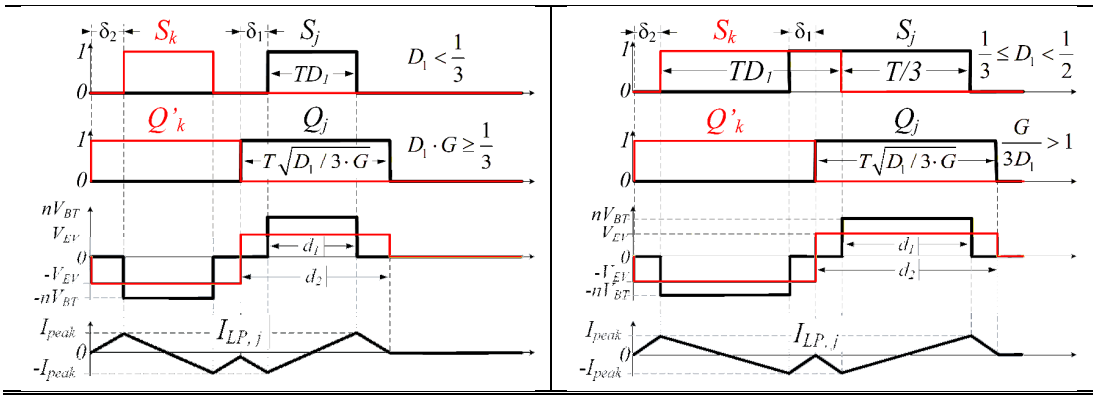


Fig. 3.4. Theoretical operation diagrams for one CF-MAB converter port, operating with mDPS modulation in different modes. Diagrams are showing primary and secondary side control signals for switches S_j, S_k, Q_j, Q'_j , primary and secondary side transformer voltages $nV_{P,j}$, $V_{S,j}$ as well as transformer current $I_{LP,j}$. Phase shift d_j in all cases equals to zero, which means no power flow to the output.

The regulation characteristics of the CF-MAB with mDPS modulation are similar to ones with a SPS modulation, that were specified previously. However, in case of mDPS, output power of the isolated ports depends not only on input side switches duty cycle D_1 and phase shift between primary and secondary voltages δ_j, but additionally on modulation variables $d_{Q,j}$, $d_{Q',j}$ and $d_{S,j}$. To obtain equations, each of eight operation modes were analyzed analytically. Average port current equations were derived by summing integrals of output current piecewise functions. Then the results were multiplied by V_{EVj} to obtain ports power P_{EVj}. Due to the fact, that form of the output current depends on the phase shift δ_j, different output power equations were obtained for each specific phase shift range (Table 3.2). Eventually, results were verified by comparing them to regulation curves obtained through modeling the converter in the PLECs software. Consequently, obtained equations were used to plot regulation characteristic for a $|\delta_j| \le 90^o$ and different D_1, G_j values (Fig. 3.5).

Table 3.2. CF-MAB converter regulation characteristics for modified DPS modulation and different modes of operation.

Mode	Phase shift d	$P_{EV,N} = \frac{V_{BT} \cdot V_{EVj}}{f_{sw} \cdot L \cdot n \cdot T^2} \cdot$
1:	$\delta_j < \lvert\delta_{Q,j}\rvert$	$d_{P,j} \le d_{S,j} \rightarrow \left[2\delta_j \cdot d_{S,j}\right]$, $d_{P,j} > d_{S,j} \rightarrow \left[2\delta_j \cdot d_{P,j}\right]$
	$\lvert\delta_{Q,j}\rvert \le \delta_j < \left(\frac{T}{3} - d_{P,j}\right) + \delta_{Q,j}$	$\left[2\delta_j \cdot d_{P,j} - (\delta_{Q,j} + \delta_j)^2\right]$
	$\left(\frac{T}{3} - d_{P,j}\right) + \delta_{Q,j} \le \delta_j < d_{P,j} - \delta_{Q,j}$	$\left[\frac{(T+3\delta_{Q,j})^2 - (T+3\delta_j)^2 - (T+3d_{S,j})^2}{18} - (\delta_j + d_{P,j}) \cdot \delta_{Q,j} + d_{P,j} \cdot \delta_j - \delta_j^2\right]$
2:	$\delta_j < \lvert\delta_{Q,j}\rvert$	$\left[2\delta_j \cdot d_{P,j}\right]$
	$\lvert\delta_{Q,j}\rvert \le \delta_j < \lvert\delta_{Q',j}\rvert$	$\left[2\delta_j \cdot d_{P,j} - (\delta_j + \delta_{Q,j})^2\right]$
	$\lvert\delta_{Q',j}\rvert \le \delta_j < d_{P,j} - \delta_{Q,j}$	$\left[2\delta_j \cdot d_{P,j} - (\delta_j + \delta_{Q,j})^2 - \frac{1}{2}(\delta_j + \delta_{Q',j})^2\right]$
3:	$\delta_j < \lvert\delta_{Q',j}\rvert$	$d_{P,j} \le d_{S,j} \rightarrow \left[2\delta_j \cdot d_{S,j}\right]$, $d_{P,j} > d_{S,j} \rightarrow \left[2\delta_j \cdot d_{P,j}\right]$
	$\lvert\delta_{Q',j}\rvert \le \delta_j < T\left(D_1 - \frac{1}{3}\right) + \delta_{Q',j}$	$\left[2\delta_j \cdot d_{P,j} - (\delta_{Q',j} + \delta_j)^2\right]$
	$T\left(D_1 - \frac{1}{3}\right) + \delta_{Q',j} \le \delta_j < \frac{T}{3} - \delta_{Q',j}$	$\frac{1}{24}\left[4\delta_j(T+3d_{S,j}) + 2Td_{S,j} - (T-2TD_1)^2 - (2TD_1 - 6\delta_j)^2 - (2TD_1 - 3d_{S,j})^2\right]$
4:	$\delta_j < \lvert\delta_{Q,j}\rvert$	$\left[2\delta_j \cdot d_{P,j}\right]$
	$\lvert\delta_{Q,j}\rvert \le \delta_j < \lvert\delta_{Q',j}\rvert$	$\left[2\delta_j \cdot d_{P,j} - (\delta_j - \delta_{Q,j})^2\right]$
	$\lvert\delta_{Q',j}\rvert \le \delta_j < \frac{T}{2} - d_{S,j} + \lvert\delta_{Q',j}\rvert$	$\left[2\delta_j \cdot d_{P,j} - (\delta_j - \delta_{Q,j})^2 - \frac{1}{2}(\delta_j + \delta_{Q',j})^2\right]$

$\frac{T}{2}-d_{S,j}+\left\|\delta_{Q',j}\right\|\le\delta_j<\frac{T}{3}+\delta_{Q,j}$	$\left[2\delta_j\cdot d_{P,j}-\left(\delta_j-\delta_{Q,j}\right)^2-\frac{1}{2}\left(\delta_j+\delta_{Q',j}\right)^2-\frac{1}{2}\left(\delta_{Q',j}+\delta_j-\left(\frac{T}{2}-d_{S,j}\right)\right)^2\right]$

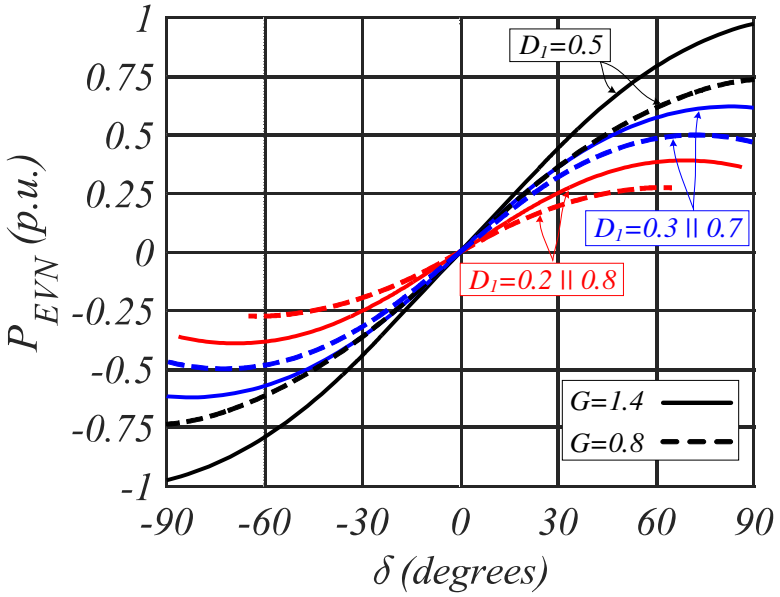


Figure 3.5. CF-MAB EV ports regulation characteristics for mDPS modulation, different D_1 and voltage mismatch ratio ($G_{j(max)}=V_{BTmax}\cdot n/V_{EVj(min)}=1400V\cdot 0.288/288V=1.4$, $G_{j(min)}=V_{BTmin}\cdot n/V_{EVj(max)}=1100V\cdot 0.288/400V=0.8$) between BT and EVs. Converter operates symmetrically regarding $D_1=0.5$, thus $D_1=m$ and $D_1=1-m$ results in the same regulation characteristics (if all other parameters are equal).

In a steady-state, operation of one isolated CF-MAB converter port can be represented by two AC sources with an inductor between them. The voltage sources instantaneous voltages are derived using Fourier series like:

$I_{LP,j}(t)$ $L_{P,j}$

$V_{P,j}(t)$ δ_j $V_{S,j}/n(t)$

$$V_{P,j}(t)=\sum_{m=1,2,3...}B_{m,BT}\cdot\sin(m\cdot\omega_0 t)$$
$$B_{m,BT}=\frac{2V_{BT}}{m\pi}\left[\cos(m\cdot\alpha_1)-\cos(m\cdot(\alpha_1+d_{P,j}))\right]$$
$$V_{S,j}(t)=\sum_{m=1,2,3...}B_{m,EVj}\cdot\sin(m\cdot\omega_0(t-\delta_j)) \quad (3.2)$$
$$B_{m,EVj}=\frac{2V_{EVj}}{m\cdot\pi}\left[\cos(m\cdot\alpha_2)-\cos(m\cdot(\alpha_2+d_{S,j}))\right]$$

where $\omega_0=2\pi f_{sw}$, α_1 and α_2 are variables from Fig. 3.7, used for waveforms derivation.

Considering that average inductor current equals to zero, $I_{LPj}(t)$ is calculated as a superposition of two currents, created by voltages $V_{P,j}$ and $V_{S,j}$:

$$I_{LP,j}(t)=\int_0^t\frac{V_{P,j}(t)-V_{S,j}(t)/n}{L_{P,j}}dt \quad (3.3)$$

From (3.2 and 3.3), instantaneous transformer inductor current is acquired:

$$
\begin{aligned}
I_{LP,j}(t) &= \sum_{m=1,2,3\ldots} \frac{2}{m^2 \omega_0 \pi L_{P,j}} \left[\sqrt{A^2 - 2AB \cdot \cos(m \cdot \omega_0 \delta_j) + B^2} \cdot \cos(m \cdot \omega_0 t + \phi) \right] \\
A &= V_{BT} \cdot \left[\cos(m \cdot (\alpha_1 + d_{P,j})) - \cos(m \cdot \alpha_1) \right] \\
B &= \frac{V_{EVj}}{n} \cdot \left[\cos(m \cdot (\alpha_2 + d_{S,j})) - \cos(m \cdot \alpha_2) \right] \\
\phi &= \arctan\left(\frac{B \cdot \sin(m \cdot \omega_0 \delta_j)}{A - B \cdot \cos(m \cdot \omega_0 \delta_j)} \right)
\end{aligned}
\tag{3.4}
$$

where α_1 and α_2 are calculated for different converter operation regions like:

Region 1: $\alpha_1 = T/3 - d_{P,j}$; Region 2, 3: $\alpha_1 = \frac{T}{2}\left(D_1 - \frac{1}{3}\right)$; Region 4: $\alpha_1 = T(1 - D_1)$,

All regions: $\alpha_2 = \alpha_1 + \delta_{Q,j}$

From (3.4), the RMS current for the transformer inductors calculated as:

$$
I_{LP,j}rms = \sqrt{\sum_{m=1,2,3\ldots} \left[\frac{\sqrt{2}}{m^2 \omega_0 \pi L_{P,j}} \sqrt{A^2 - 2AB \cdot \cos(m \cdot \omega_0 \delta_j) + B^2} \right]^2}
\tag{3.5}
$$

Important to note, that all harmonics present in the current and voltage waveforms. For CF-MAB with SPS modulation, equations described above are the same, but $\alpha_1 = \alpha_2$, $d_{P,j} = d_{S,j}$. For a typical conventional single-phase DAB converter with SPS modulation $\alpha_1 = \alpha_2 = 0$, $d_{P,j} = d_{S,j} = 0.5T$.

To verify the obtained formulas for the mDPS from the table 3.2, switching model of the converter were implemented in PLECs software. Simulation results (Figure 3.6) show different converter operation intervals under varying EV currents for both SPS and mDPS modulation: t_0 - BT is transferring power both to EVs and DC grid; t_1 – both BT and DC grid power EVs; t_2– BT and EVs are charged from DC grid; t_3 –EV_2 and DC grid send energy to EV_1 and EV_3; t_4 – EV_2 delivers power to EV_1, EV_3 and DC grid; t_5 – BT charged from DC grid and EV_2 transfers power to EV_1.

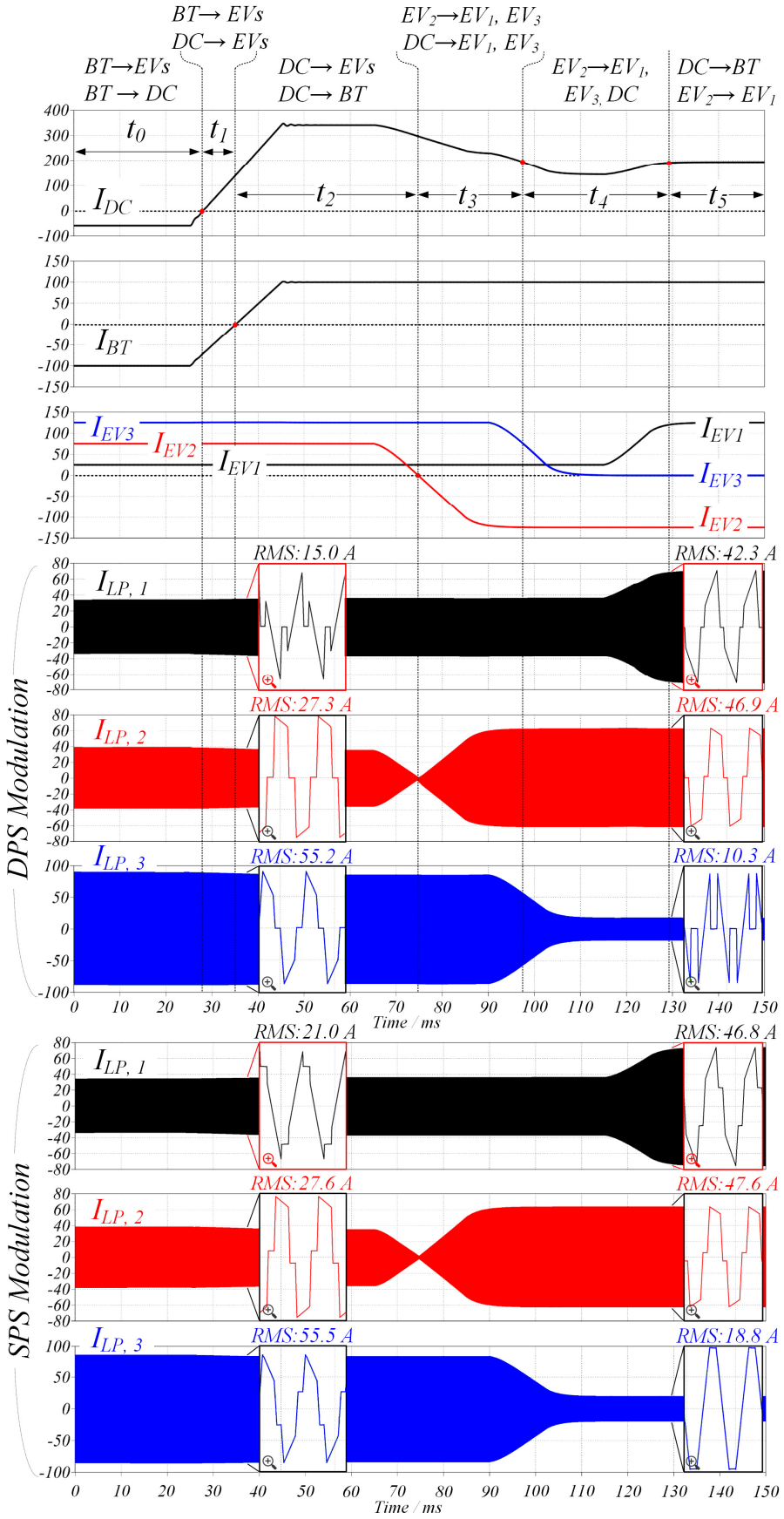


Figure 3.6. Simulated converter operation diagrams for $N=3$ during change of EV charging current for system parameters: V_{BT}=1200V, V_{DC}=600V, V_{EV1}=288, V_{EV2}=345V, V_{EV3}=400V. Transformer currents are shown for both DPS modulation (a) and SPS modulation (b). In the diagrams, several possible power flow directions between BT, EV and DC grid are shown, which occur on the specified intervals.

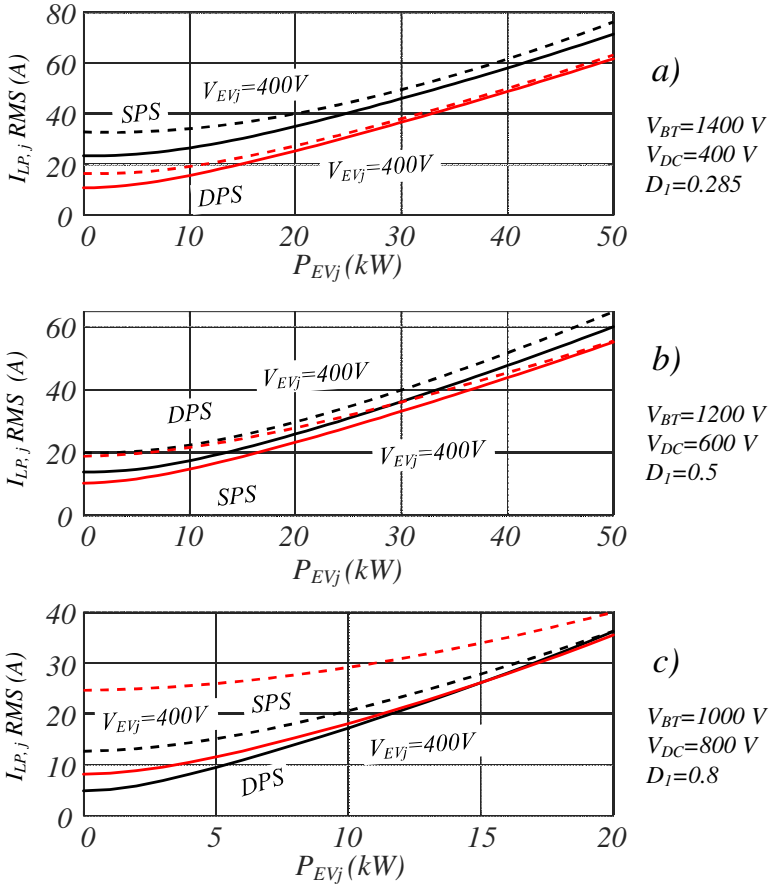


Figure 3.7. Comparison of RMS currents for SPS and mDPS modulations for different scheme conditions: a) Low D_1 when storage battery has high SOC and DC grid voltage is low; b) Medium D_1 when both storage battery and DC grid at their nominal voltages; c) High D_1 when storage battery is discharged and DC grid voltage is high. Relations are built using equations (3) and verified using simulation.

The results obtained during the simulation and theoretical calculations (equation 3.5) coincide, showing mDPS lower RMS currents in comparison to the SPS modulation in the whole range of power and different V_{DC} / V_{BT} ratios (Figure 3.7). Important to note, that the higher the voltage mismatch between EV and BT, the higher the impact of the mDPS modulation on the RMS current is observed for all studied cases. For example, during case b), for V_{EV}=400V (G=0.86) transformer RMS current reduction is only 1.8%, whereas for higher mismatch of V_{EV}=288V (G=1.2), the decrease is already 7.7%. A similar situation is observed for a) and c) cases. RMS current for G=1 is not shown, because SPS and mDPS in such cases almost become the same and there is no big difference in RMS currents. Overall, an average RMS current reduction of 5.7% was observed for a), b) and c) cases during peak power delivery and 43.6% RMS current reduction during zero power delivery.

It is important to point out, that for the case c), the maximum power delivered to the EV is much lower than for cases a) and b), which is explained by low battery voltage and simultaneous high D_1, which results in an input side transformer voltage having both low amplitude and duration d_1. Thus, current through the transformer cannot reach a value high enough to deliver 50kW. To overcome it, transformer leakage inductance L_{Pj} can be increased, but according to equation 3.5 it would increase RMS currents for all other regimes. Since c) is an extreme case, which is not likely to occur during system normal operation, it is better to limit power delivery during it to some value (20kW in the studied case). Moreover, cases a) and c) in Fig.3.7 show extreme converter operation regimes, where traction grid voltage changes in a range of ±200V and I_{BT}=0, which means, no DC grid voltage stabilization is provided, resulting in a D_1 changing in a range of 0.285...0.8. However, DC grid voltage stabilization, provided by the BES allows reducing ΔV_{DC} and consequently D_1 change range, avoiding power reduction cases as in c). However, for the purity of the experiment, all possible modes that cover the full voltage range of the traction grid and BT are shown in the study.

4. Converter control algorithm.

Converter control can be split into two main parts: the high-level control algorithm, which forms reference BT and EV currents based on the traction grid catenary voltage V_{CT}, and low level control, which ensures that reference values I_{BT}^{ref}, $I_{EV\,N}^{ref}$ passed from high level control are maintained, using closed loop control.

A. Buffer battery SOC balancing.

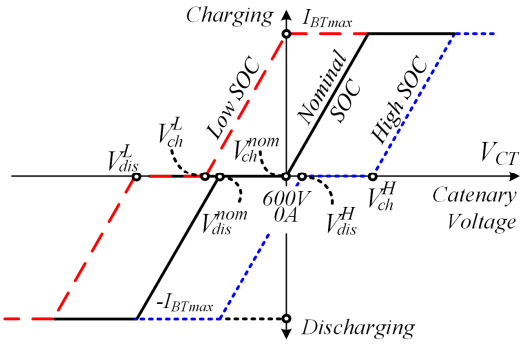


Figure 4.1. Buffer battery charge/discharge characteristic, depending on the battery state of charge SOC_{BT}.

Converter BT and EVs charging and discharging are catenary voltage-based, where voltage V_{CT} is the factor that defines system state. When catenary voltage rises above some charging level V_{ch}, buffer battery BT starts charging, and when voltage drops below some discharging level V_{dis}, BT dischargers. Such a behavior allows reducing catenary voltage sags related to transit transport acceleration and recuperate braking energy during transport braking, lowering voltage surges. During converter operation, BT state of charge (SOC) changes, which is related to different recuperated and supplied to the grid power levels. In conventional traction wayside energy storages, simple balancing method, that adjusts V_{ch} and V_{dis}, to keep SOC_{BT} at its nominal state is used (Fig. 4.1)**¡Error! No se encuentra el origen de la referencia.**. Thus, to keep SOC_{BT} at the nominal level of SOC_{BT}^{nom}, limits are adjusted in the following way:

$$V_{ch} = \frac{\left(SOC_{BT} - SOC_{BT}^{nom}\right)\cdot\left(V_{ch}^{H} - V_{ch}^{L}\right)}{SOC_{BT}^{\max} - SOC_{BT}^{\min}} + V_{ch}^{nom}$$
$$V_{dis} = \frac{(SOC_{BT} - SOC_{BT}^{nom})\cdot(V_{dis}^{H} - V_{dis}^{L})}{SOC_{BT}^{\max} - SOC_{BT}^{\min}} + V_{dis}^{nom} \quad (4.1)$$

where SOC_{BT}^{nom} – nominal BT SOC, which is typically kept at the level of 50%, to have capacity for both charge and discharge; SOC_{BT}^{max}, SOC_{BT}^{max} – maximum/minimum battery SOC; V_{ch}^{H}, V_{ch}^{L} – catenary voltage charging thresholds for high and low BT SOC correspondingly; V_{dis}^{H}, V_{dis}^{L} – catenary voltage discharging thresholds for high and low BT SOC; V_{ch}^{nom}, V_{dis}^{nom} – nominal charging/discharging thresholds when BT SOC is at SOC_{BT}^{nom} level.

Thus, when battery SOC is low, charging and discharging occur at lower voltages V_{ch}^{L} and V_{dis}^{L}, rather than nominal V_{dis}^{nom} and V_{ch}^{nom}, making the battery harder to discharge. This ensures that higher portion of power for the tram is supplied by the substation rather than the battery, which would also cause voltage V_{CT} to drop to a lower level. The same happens when BT is at high SOC, where the limits are increased to V_{ch}^{H} and V_{dis}^{H}, making BT harder to charge. In addition, when traction line is not loaded and its voltage V_{CT} at the nominal level, the BT is charged or discharged, until it reaches SOC_{BT}^{nom}.

Limits adjustments, described by (4.1) assume, that when no traction transport is operating on the line, the catenary voltage is at known level and is close to the output voltage of the substation ($V_{CT} \approx V_{DC}$). However, when EVs are charging, the catenary voltage decreases ($V_{CT}^{EVs} < V_{DC}$), meaning that SOC balancing is disrupted, as the voltage of the line can no longer rise to its nominal value. This causes SOC_{BT} to stabilize at a level below the nominal value. Thus, V_{ch}^{nom} has to be lowered to the level of V_{CT}^{EVs}, to maintain voltage balancing. However, the situation is complicated by the fact that number of connected EVs changes, as well as power consumption of each individual EV charger. This causes the catenary voltage drop. The voltage drop varies within a range, starting from zero, when no EVs are parked, to the maximum voltage value when all ports are charging EVs at maximum power. Thus, to achieve BT SOC balancing at a defined level SOC_{BT}^{nom}, regardless of the EV load, V_{ch}^{nom} and V_{dis}^{nom} must be adjusted by a value V_{adj}:

$$V_{ch}(i) = V_{adj}(i) + V_{ch}^{nom},\ V_{dis}(i) = V_{adj}(i) + V_{dis}^{nom}, \quad (4.2)$$

where $V_{adj}(i)$ is regulated based on the proportional-integral (PI) controller:

$$V_{adj}(i) = V_{adj}(i-1) + e_{SOC}(i-1)\cdot(0.5\cdot ki\cdot T_{SOC} - kp) + \\ + e_{SOC}(i)\cdot(0.5\cdot ki\cdot T_{SOC} + kp), \quad (4.3)$$

$$e_{SOC}(i) = SOC_{BT}(i) - SOC_{BT}^{nom}, \quad (4.4)$$

where *kp* – proportional gain, *ki* – integral gain, T_{SOC} – SOC measuring period, e_{SOC} – SOC error.

The maximum adjustment value V_{adj} should be limited to a range [$-V_{adj}^{max}$: V_{adj}^{max}] to prevent situations where V_{ch} and V_{dis} are shifted too close to the lowest V_{CT} limit (according to standard EN 50163). On the other hand, V_{adj}^{max} must be high enough to ensure stable battery SOC balancing when the catenary is fully loaded with EVs. Therefore, the adjustment voltage should not be limited to a value lower than ($V_{CT} - V_{CT}^{EVsmax}$), where V_{CT}^{EVsmax} is the value corresponding to the maximum number and power of connected EVs.

B. High level control algorithm

The control algorithm starts by measuring all necessary system parameters as voltages V_{CT}, V_{BT}, $V_{EV\,N}$, currents I_{BT}, $I_{EV\,N}$ and calculating the catenary thresholds V_{dis} and V_{ch} (Fig. 4.2). Then, the voltage of the traction gird V_{DC} is compared to these thresholds and is made on whether BT should charge, discharge or remain int the IDLE state, considering the minimum BT voltage V_{BTmin} and maximum voltage V_{BTmax}. For example, when battery needs to be discharged, but the battery voltage is below V_{BTmin}, the BT is staying in the IDLE state with $I_{BT}^{ref} = 0$, instead of discharging further. The same principle applies for BT charging if the higher charging limit V_{BTmax} is exceeded, the reference battery current is set to $I_{BT}^{ref} = 0$. In the case where the battery operates within the range of $V_{BTmin}<V_{BT}<V_{BTmax}$, the charging/discharging reference currents are defined by equations (4.5), respectively. When the voltage of the DC grid is within the range $V_{dis}<V_{CT}<V_{ch}$, the battery is kept in the IDLE state with $I_{BT}^{ref}=0$ as well. The coefficient k_{BT} is a droop coefficient that defines max voltage difference $\Delta V_{CT\,max}$ between the start and end of the stabilization process.

$$BT\ charging: I_{BT}^{ref} = (V_{CT} - V_{ch})\cdot k_{BT}, \\ BT\ discharging: I_{BT}^{ref} = (V_{CT} - V_{dis})\cdot k_{BT}, \quad (4.5)$$

where $k_{BT} = I_{BTmax}^{ref} \cdot \Delta V_{CTmax}$.

In all the aforementioned BT states, the charging behavior of the EVs is different and depends on the catenary voltage. In the simplest case, when $V_{CT} > V_{dis}$, EVs charge with the maximum allowable current I_{EVmax}^{ref}, following CC/CV profile. When voltage $V_{CT} < V_{dis}$, EVs start operating with a smart charging algorithm, where reference charging current I_{EV}^{ref} is calculated using the next formula:

$$I_{EV\,N}^{ref} = I_{EVN\,\max}^{ref} + (V_{CT} - V_{dis})\cdot k_{EV} \quad (4.6)$$

where $k_{EV} = I_{EVmax}^{ref} \cdot \Delta V_{CTmax}$.

According to (4.6), the EV current is regulated based on the the catenary voltage V_{CT} with a droop coefficient k_{EV}. The current distribution between EVs and BT during discharging can be changed, by modifying the relation between k_{EV} and k_{BT}. This paper discusses the case, when k_{EV} and k_{BT} are equal. This means that during low V_{CT} voltage drops, EVs operate with a smart charging, reducing consumption depending on the (V_{CT} - V_{dis}) difference, and discharging in cases where the line load increases significantly, causing (V_{CT} - V_{dis}) to drop below a certain level. Also, important to note, that all condition blocks in the control system, which define system states, operate with hysteresis to avoid states oscillations.

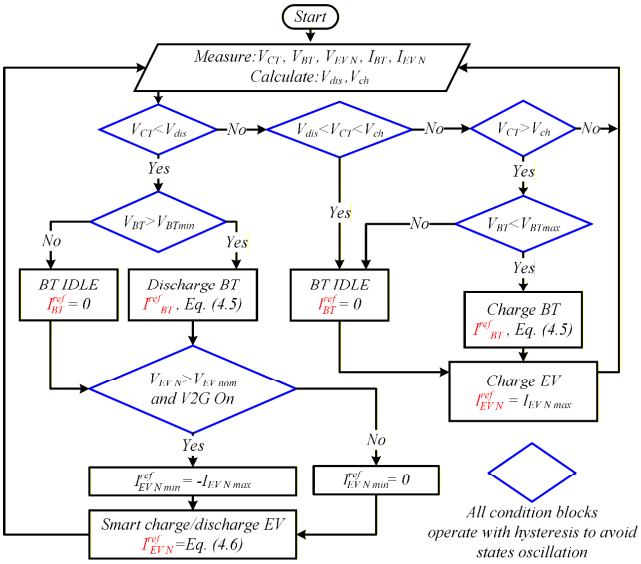


Figure 4.2. Catenary-based system high level control algorithm, that shows how reference battery I_{BT}^{ref} and EVs $I_{EV\,N}^{ref}$ currents are formed.

C. Low level control system

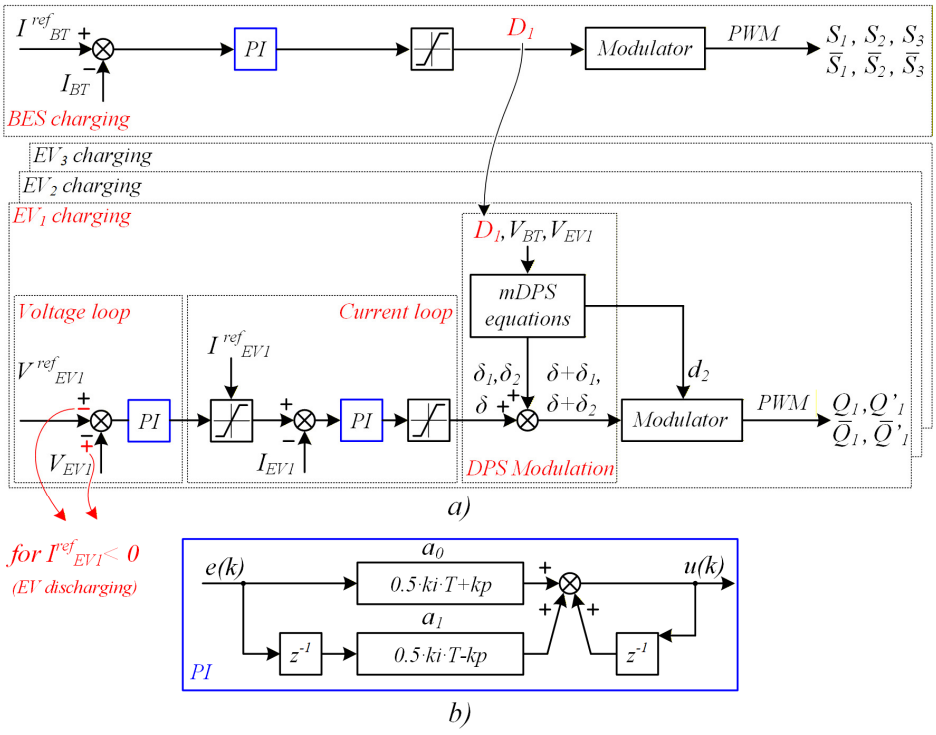


Figure 4.3. a) Low level system control, which takes reference currents I_{BT}^{ref} and $I_{EV\,N}^{ref}$ as inputs from high-level control and, in a close loop manner, maintain those values by changing input side duty cycle D_1 and each EV port phase shift δ; b) structure of digital PI controllers in the control system.

EVs charging/discharging is based on a constant-current/constant voltage (CC/CV) algorithm, which is one of the most common in EV charging applications. Since BT is maintained at a mid-level charge by described balancing algorithm, ensuring capacity for both charging and discharging when needed, there is no necessity for a CV charging mode and voltage regulator in the control system for the BT. Thus, BT current I_{BT} is adjusted using a single PI controller, which regulates the charging current by comparing measured I_{BT} with the reference I_{BT}^{ref} and

accordingly adjusting D_1 (Fig. 4.3a). Nevertheless, the battery V_{BTmin} and V_{BTmax} voltages are monitored during converter operation by the high-level control and charging/discharging is stopped, when limits are crossed. CC/CV charging is achieved using typical two-stage voltage and current loops, where the difference between reference currents/voltages $I_{EV\,N}^{ref}$, $V_{EV\,N}^{ref}$ and measured ones I_{EVN}, V_{EVN} is fed to the corresponding PI controllers, which generate a phase shift φ for each port. This two-stage control allows smooth transition from CC to CV mode. When switching from charging to discharging modes, the signs of $V_{EV\,N}^{ref}$ and $V_{EV\,N}$ are reversed to make the output of voltage PI controller negative, ensuring the correct operation of the subsequent saturation block with the $I_{EV\,N}^{ref}$ limit. The control also implements dual-phase shift (mDPS) modulation, which matches volt-seconds on the primary and secondary sides of the transformer to reduce the flowing RMS current. As inputs, the mDPS modulation takes D_1, V_{BT} and $V_{EV\,N}$ and generates corresponding phase shifts δ_1 and δ_2 for the full bridge arms, which are then added to the base phase shift δ and fed to the modulator, along with an updated output side duty cycle d_2. All PI controllers in the control system are digital controllers in z domain (Fig. 4.3b), derived from the s domain PI controller transfer function by using bilinear transform.

D. Hardware in the loop tests

To verify converter control, described in section III, HIL simulation of the CF-MAB converter with 3 EV ports, BT and DC grid was performed. The HIL simulation setup consists of a PLECS RT Box 1, which simulates converter hardware, and a Delfino TMS320F28379D control card from Texas Instruments. At its analogue outputs, the RT Box generates signals, proportional to the measured converter voltages and currents, which are then sampled by the TMS320F28379D analogue to digital converters. The controller then processes the control algorithm described in the previous section and generates corresponding PWM signals for the transistors. These PWM signals are then sampled by RT BOX digital input channels with a 7.5 ns sampling rate, averaged and updated in the model with a discretization step of 8us. The nominal converter operating switching frequency is 25kHz. However, since the model averages signals over an 8us interval, the switching frequency is reduced by a factor 10, down to 2.5 kHz, to better track and debug the low-level system control operation. The most important model parameters are specified in Table 4.1. Since the converter operates at a frequency 10 times lower than nominal, inductor and capacitor values are increased 10 times in comparison to the calculation for 25 kHz of the switching frequency.

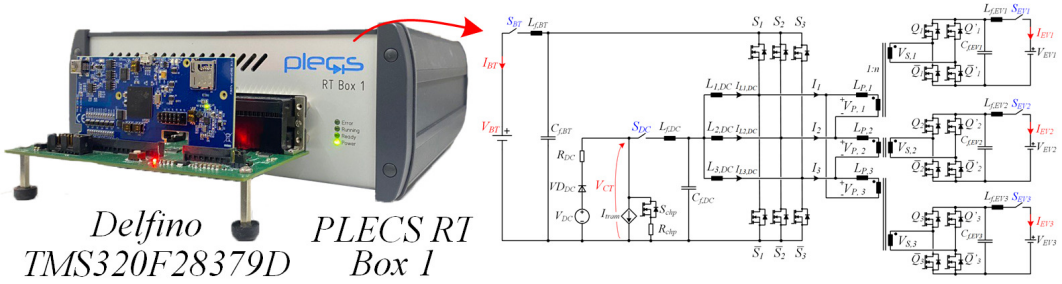


Figure 4.5. HIL setup with a PLECS RT BOX 1 as a CF-MAB hardware simulator and Delfino TMS320F28379D controlCARD R1.3 as a control board, and the simulated circuit with N=3.

Table 4.1. CF-MAB HIL Model Parameters.

Parameter	Value
DC grid voltage V_{DC}	600 V
DC grid resistance R_{DC}	0.2 Ohm
Battery nominal voltage V_{BT}^{nom}	1200 V
Battery capacitance C_{BT}	10.5 Ah
Battery resistance R_{BT}	0.1 Ohm
Battery maximum current I_{BT}^{max}	250 A
EV voltage V_{EV1}, V_{EV2}, V_{EV3}	345 V
EV maximum current I_{EV1}^{max} , I_{EV2}^{max} , I_{EV3}^{max}	125 A
Transformer ratio *1:n*	0.28
DC side inductance $L_{1,DC}$, $L_{2,DC}$, $L_{3,DC}$	10•50 uH
Primary inductance $L_{P,1}$, $L_{P,2}$, $L_{P,3}$	10•30 uH
Battery side capacitor $C_{f,\,BT}$	10•470 uF
Battery and EV sides inductances $L_{f,\,BT,}$ L_{fEV}	10•10 uH
EV side capacitor C_{fEV}	10•1 mF
DC filter inductance $L_{f,DC}$	8 uH

DC filter capacitor $C_{f,DC}$	4 mF
Discretization step size, *Tstep*	8 us
Switching frequency f_{sw}	2.5 kHz

The DC grid voltage is set as a constant voltage source V_{DC} with a series diode to block reverse power flow to the substation. It is assumed, that the tram operates at some distance from the substation. At the same location, CF-MAB converter with a buffer battery is connected. R_{DC} represents resistance of the traction catenary, which causes voltage drop on the line due to tram and EV charger operation. Tram is simulated as a constant current source, controlled to maintain considered tram power profile (Fig. 4.6). The peak tram braking power is considered to be at the level of -150kW, which causes catenary voltage to rise. When the voltage reaches V_{CT}=*800V,* the braking chopper engages (S_{chp}, R_{chp}, Fig. 4.5), limiting further increases in catenary voltage. During tram acceleration with a peak consumption of 400kW, typical for a medium size tram, V_{CT} drops to a level of 400V. The model also includes relays S_{BT}, S_{DC}, S_{EV1}, S_{EV2}, S_{EV3} which close after port capacitors are pre-charged.

The main task of HIL simulation is to demonstrate the operation of the BT and EVs during changes in P_{tram} and compare the two BT SOC balancing algorithms described earlier, using the parameters from Table 4.2. To achieve this, the tram profile shown in Fig.4.6 is continuously repeated over 10 minutes to observe how it affects the BT SOC. The battery capacity was intentionally lowered to 10.5 Ah, which is lower than typical value for a wayside energy storage, to better observe SOC changes. The simulation was conducted for three cases: 1) no power consumption from EVs $I_{EVN} = 0$; 2) EVs consume 1/5 of their peak current $I_{EVN}=I_{EV}^{max}/5$; 3) EVs consume peak power $I_{EVN} =I_{EV}^{max}$ (Fig. 4.7).

Table 4.2. Main BT SOC balancing parameters.

Parameter	Value
Nominal charging voltage V_{ch}^{nom}	600 V
Nominal discharging voltage V_{dis}^{nom}	575 V
Maximum adjastable voltage V_{adj}^{max}	75 V
Nominal state of Charge V_{BT}^{nom}	50%
Maximum voltage difference of caternacy ΔV_{CTmax}	25 V
Droop battery coefficient $k_{BT,}$ droop EV coefficient k_{EV}	10

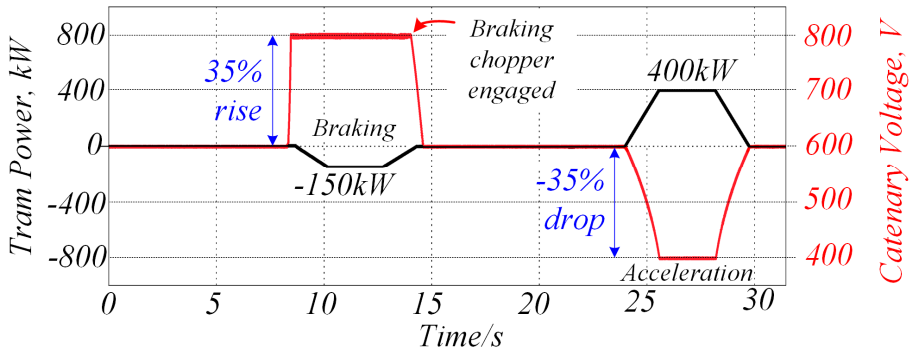


Figure 4.6. Simulated tram power profile P_{tram} and its affect on the catenary voltage V_{CT}.

The simulation results (Fig. 4.7) show that the implementation of conventional BT SOC balancing control leads to the stabilization of the BT SOC close to 50% for cases in Fig. 4.7 a) and 4.7 b), where the EVs load on the line is not significant. It is clearly observed that for both cases in Fig. 4.7 a) and 4.7 b), during zero power consumption by the tram, the BT charges, increasing its SOC. However, in the third case, Fig. 4.7 c), where higher EVs consumption is present, the BT SOC decreases over time, and the BT is not charged even when no tram is on the line. This is caused by the fact that the catenary voltage, with EVs being charged, is lowered to a value V_{CT}^{EVsmax}, which is close to V_{ch}^{L}. As a result, the BT only starts charging when its SOC drops to a low level, eventually stabilizing at the low BT_{SOC}^{min} level, which is set to 20%. Consequently, for different catenary loads, the BT SOC stabilization level varies. In contrast, the adjustable limits, simulated with cases shown in Fig. 4.7 d), 4.7 e) and 4.7 f) show that the battery SOC is stabilized in all cases, regardless of EVs consumption. The balancing time is slightly different in each of the three cases, as during EV charging, a higher portion of the recuperated energy from the DC grid is used for EV charging instead of BT charging. In all the aforementioned cases, all EVs operate in the constant current region, following the same smart charging control, reducing the charging current during tram acceleration to minimize the V_{CT} voltage drop.

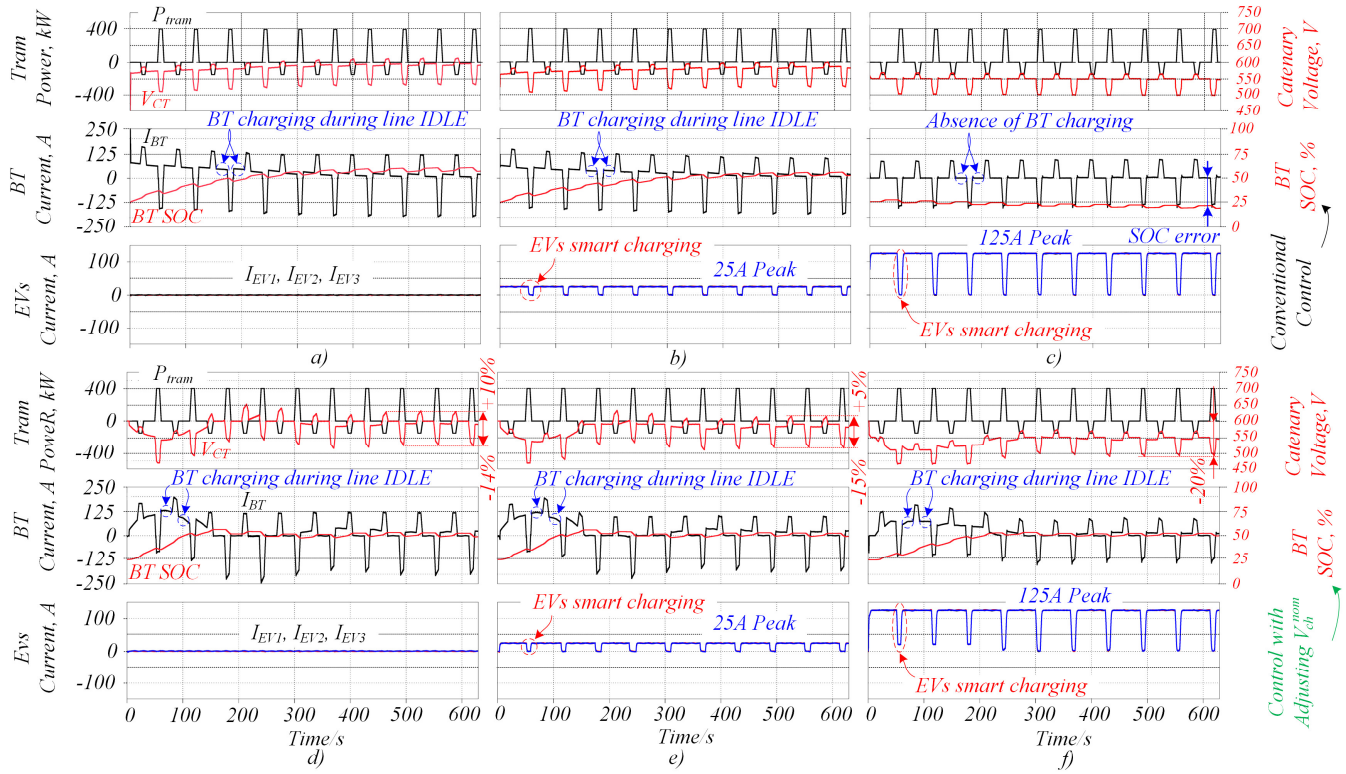


Figure 4.7. HIL simulation results for two BT SOC balancing controls – the conventional one, which does not take into account V_{CT} decrease caused by EVs load (a, b, c), and the improved one with a controller that adjusts V_{adj} (d, e, f). The simulation for all cases was conducted for a 60 seconds tram cycle period, fitting 10 cycles in 600 seconds simulation time. Tram power profile is the same in all cases and follows the profile in Fig. 4.6.

5. Experimental verification of the results.

Primary side boost inductors value $L_{j,DC}$ is determined by the maximum allowable ripple r for the specified maximum power $P_{DC(max)}$:

$$L_{j,DC(CF-MAB)} \geq \frac{3 \cdot V^2_{DC(\max)} \left(1 - \frac{V_{DC(\max)}}{V_{BT(\min)}}\right)}{r \cdot P_{DC(\max)} \cdot f_{sw}} \tag{5.1}$$

where $P_{DC(max)}=P_{BT(max)}+N \cdot P_{EVj(max)}$, N-number of EV ports.

When it comes to $L_{P,j}$ value, its must be low enough to deliver peak desired power $P_{EVj(max)}$ to the output during the worst case scenario and maximum desired phase shift $\delta_{j(max)}$. Usually, for a DAB converters $|\delta_{j(max)}| \sim \pi/6$:

$$L_{P,j(CF-MAB)} \leq \frac{V_{EV,j(\min)} V_{BT,j(\min)}}{2n \cdot \pi \cdot f_{sw} \cdot P_{EVj(\max)}} \delta_{j(\max)} \left(\frac{2}{3} - \frac{|\delta_{j(\max)}|}{2\pi}\right) \tag{5.2}$$

The analytically derived equation (5.2) is accurate only for a specific range of ($|\delta_{j(max)}|<2\pi(1/3-D_1)$) $\cup$ ($0<|\delta_{j(max)}|<2\pi(D_1-1/3)$) and SPS modulation. Outside this range, the equation changes slightly due to variations in $d_{P,j}$ and the transformer current waveform change. This leads to an increase in the minimum $L_{P,j}$ value or, alternatively, higher phase shift $|\delta_{j(max)}|$ to achieve the desired power. For equations covering all converter operating regions and for operation with modified DPS modulation, please refer to reference.

To verify converter operation, smaller scale prototype was assembled with the components specified in Fig. 5.1 and Fig. 5.2, and parameters from Table 5.1.

Table 5.1. CF-MAB converter Prototype Parameters.

Parameter	Value
DC grid voltage range V_{DC}	200-450 V
Battery Voltage V_{BT}	600 V
EVs voltage range V_{EV1}, V_{EV2}, V_{EV3}	250-350 V
Transformer ratio n_s/n_p	0.5
Primary side turns number n_p	28
Secondary side turns number n_s	14
Transformer magnetizing inductance	45 mH
Transformer leakage inductance	10 uH
DC side inductance $L_{1,DC}$, $L_{2,DC}$, $L_{3,DC}$	490 uH
$L_{1,DC}$, $L_{2,DC}$, $L_{3,DC}$ number of turns	23
Primary transformer inductors $L_{P,1}$, $L_{P,2}$, $L_{P,3}$	100 uH
$L_{P,1}$, $L_{P,2}$, $L_{P,3}$ number of turns	11
Inductors $L_{1,DC}$, $L_{2,DC}$, $L_{3,DC}$, $L_{P,1}$, $L_{P,2}$, $L_{P,3}$ air gap	4 mm
Battery side capacitor $C_{f,BT}$	2x420 uF
Battery and EV sides inductances $L_{f,BT}$, L_{fEV}	10 uH
EV and DC side capacitors C_{fEV}, C_{fDC}	420 uF
Filter inductance $L_{f,DC}$	10 uH
Switching frequency f_{sw}	25 kHz

a) b)

Figure 5.1. Developed full bridge module, used for converter assembling (a), and converter magnetics (b). For the input side

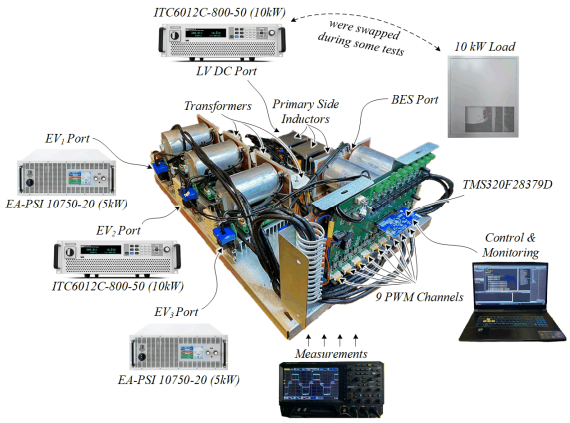


Figure 5.2. Assembled CF-MAB converter prototype, tested with up to 10kW, and the equipment used.

3-phase full bridge, same modules are used as in (a), but with 3 transistor half-bridge modules.

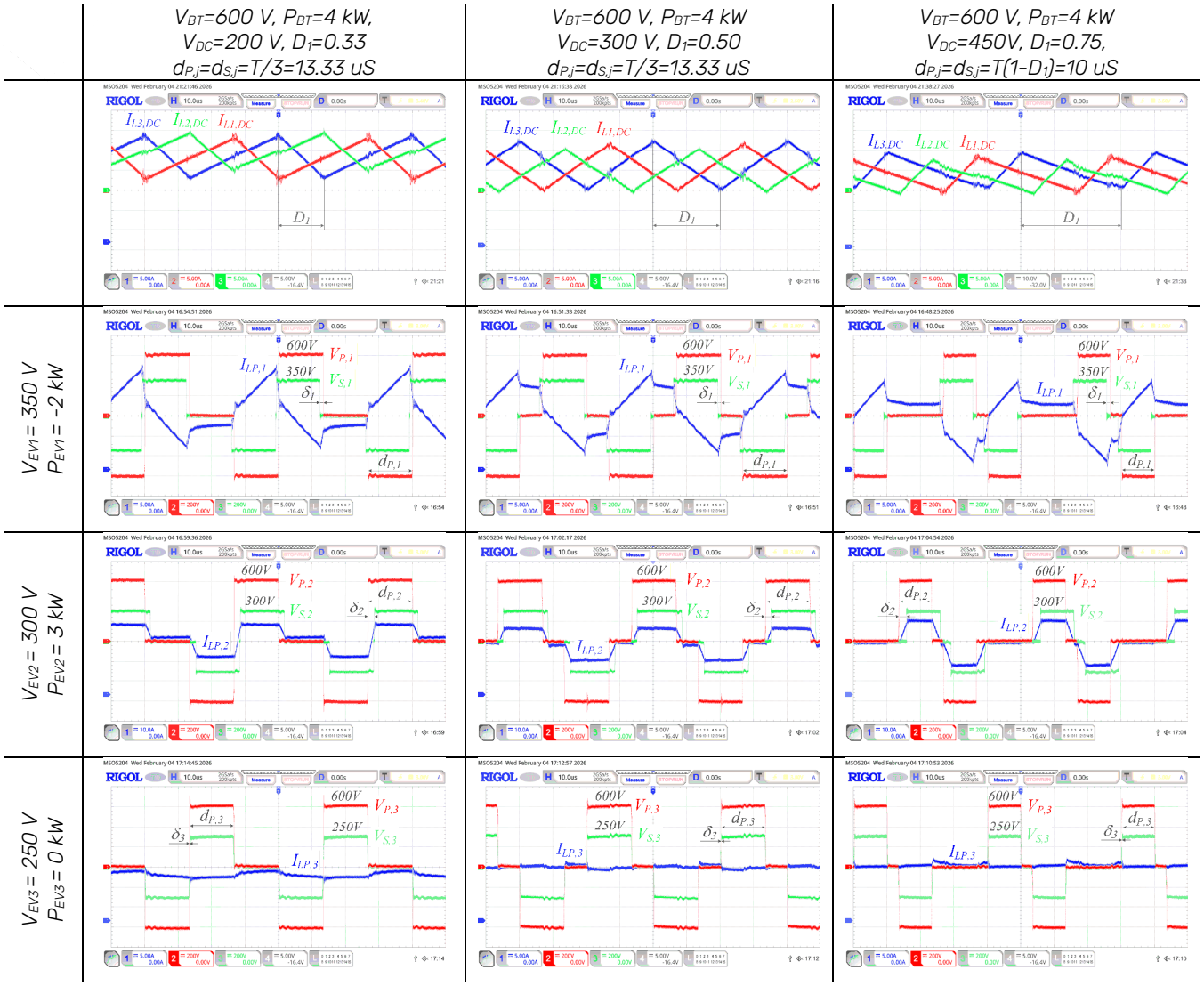


Figure 5.3. Measured waveforms of the converter operation for different operating conditions. Battery port voltage V_{BT} in all cases were held constant, as in a practical aplication, it does not change fast and depends on SOC. Converter operation is shown for different DC grid V_{DC} voltage, which represents changes of traction grid voltage, that usually occur in real operating conditions. Power and voltage of each EV is also different, to show how operating waveforms change during different conditions. The EV_3 port power is zero and EV_3 is disconnected with the relay, but still, current flows throug a transformer.

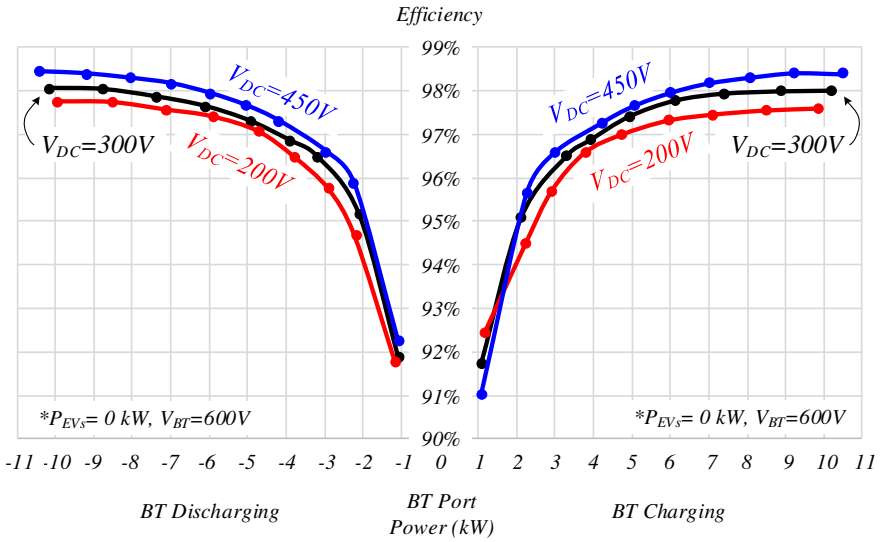


Figure 5.4. Efficiency curves for zero EVs charging power P_{EVs}=0kW and different DC grid voltage V_{DC}.

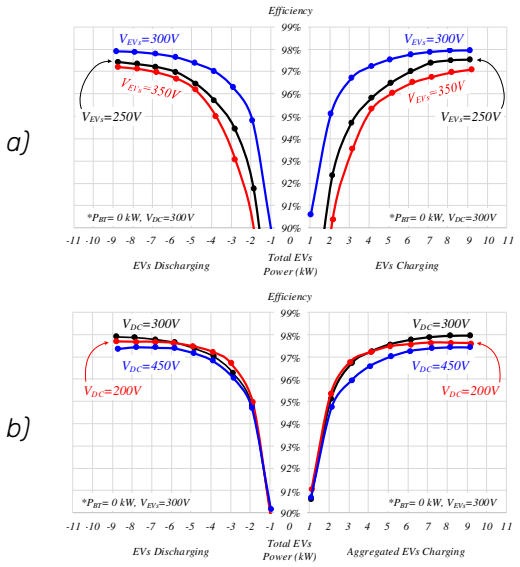


Figure 5.5. Efficiency curves for zero BT charging power P_{BT}=0kW and different V_{EVs} voltage, while DC grid voltage is constant V_{DC}=300V (a), as well as different DC grid voltage V_{DC} while all EVs voltage is the same and equals to V_{EVs}=300V (b). Power is equally shared between 3 EV ports.

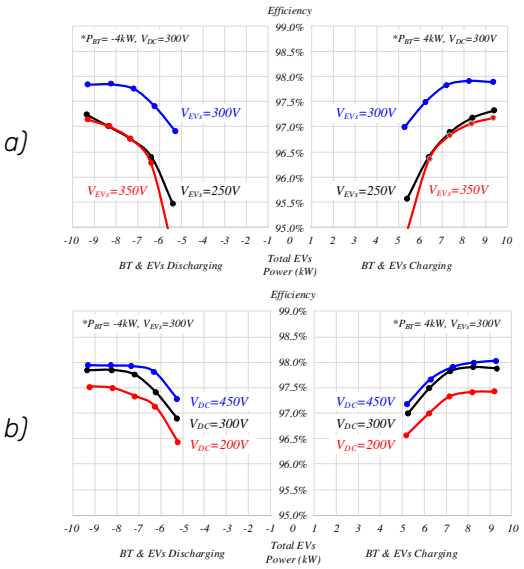


Figure 5.6. Efficiency curves when both EVs and BT is charging or discharging for different EVs voltage levels, while DC grid voltage is constant V_{DC}=300V (a), and different DC grid voltage levels, while all EVs voltage is the same and equals to V_{EVs}=300V (b). Charging and discharging power of the BT port in all cases is constant and equal to P_{BT}=±4kW, where sign depends on wether battery is charging or discharging.

When only the BT port operates and EV ports power is zero P_{EVS}=0, efficiency is highest at a high input voltage (V_{DC}=*450V*), due to lower input current and reduced ohmic losses (Fig. 5.4). However, when power is delivered only to EVs and P_{BT}=0, the situation reverses: the lowest efficiency occurs at V_{DC}=450V (Fig. 5.5b), because of lower d_{Pj}, reduced transformer utilization and increased transformer RMS currents. The highest efficiency is achieved when the battery voltage V_{BT}=600V matches V_{EVs}=300V using a transformer with a ratio of n_s/n_p=0.5 (Fig. 5.5a).

When both EV and BT ports are loaded and V_{DC}=*300V*, the highest efficiency occurs for V_{EVs}=*300V*, because the EV ports voltage is matched with the battery voltage. For V_{EVs}=*250V* or *350V*, transformer circulating currents increases and efficiency drops by about 1% (Fig. 5.6a). In Fig. 5.6b, the low EV-port efficiency at V_{DC}=*450V* is compemsated by high input-side efficiency, keeping the overall efficiency high.

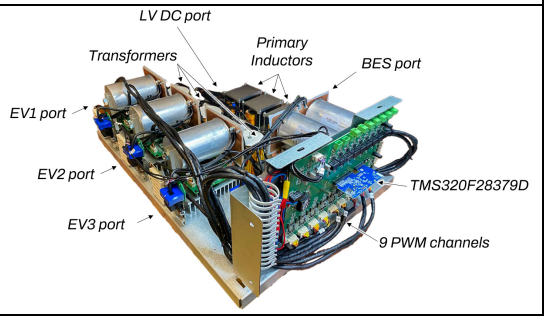
3.2.3. Contribution to the WP objectives

Main results of a research are a proposed connection scheme together with a control algorithm, which complies with the working package objectives 2, 3 and 4. In particular:

- The proposed multiport CF-MAB converter topology allows optimization of power distribution among system components (BT, EVs and the LV DC traction grid), reducing losses and improving DC grid power quality. At the same time, while providing the same functionality, the proposed converter requires a reduced number of components (6N vs. 8N + 6 required for conventional independent converter connections, where N is the number of connected EVs). The reduced number of components results in approximately 10% lower total device rating and lower installation cost. Despite having fewer components, the CF-MAB converter also provides a shorter energy conversion path between units (compared to independent converter connections), which results in higher efficiency.
- Analysis of the CF-MAB converter modulation techniques has shown that the default single-phase shift (SPS) modulation results in increased transformer RMS currents and reduced efficiency, particularly when the voltages of the BT port and EVs are not perfectly matched. Therefore, the modified dual-phase shift (mDPS) modulation for the studied converter was described and implemented to achieve volt-second balance across the transformer leakage inductor. The implementation of mDPS resulted in an average RMS current reduction of approximately 5.7% compared to SPS modulation at the nominal power level under different operating conditions. However, at lower power levels, mDPS modulation showed a more significant improvement, reducing RMS currents by approximately 43.6% on average.
- The developed high-level converter control algorithm enables the utilization of EV batteries and an additional storage battery as flexible components of a smart grid by providing bidirectional charging as well as V2G and V2V operation. The system enhances the power quality of a low-voltage DC grid by providing grid voltage stabilization, optimized power flow among system participants and improved efficiency through the recuperation of traction transport braking energy. Verification of the developed control was carried out using real-time hardware-in-the-loop (HIL) tests with a PLECS RT Box 1. HIL tests of the converter at a nominal power level of 400 kW demonstrated the system's ability to completely eliminate voltage surges caused by traction transport braking, as well as reduce voltage drops from –33% to only –12.5% through the aggregated discharging of the battery storage and EVs (peak tram power during the test was 400 kW, while peak recuperated energy reached 250 kW).
- Experimental verification, conducted using a smaller-scale converter prototype, demonstrated its ability to independently deliver power to any port without affecting the power of other ports. In practice, this means that the BT and EVs can be independently charged or discharged and their power levels can be regulated without influencing the other ports, which distinguishes the studied converter from typical multi-active bridge converters with a common transformer core. The converter demonstrated a high peak efficiency of 98% at 9.5 kW when the EV voltage (V_{EVs}=300V) is matched with the BT voltage (V_{BT}=600V) using a transformer with a turns ratio of n=0.5. During voltage mismatch conditions (V_{EVs}=250V or V_{EVs}=350 V), the efficiency decreases due to increased RMS currents in the transformer and switching devices.

3.2.4. Scientific achievements

Experimental prototypes

#	Name	Description	Status (designed, assembled, tested)	Photo
1	Five Port Current-Fed Multi-Active Bridge Converter	20kW prototype was assembled at the facilities of GUT.	Designed, assembled & tested	

Publication

#	Title, incl. citation information	Type (Conference, journal, book chapter)	Status (Submitted, accepted, published)	DOI
1	I. Verbytskyi, M. Lukianov, K. Nassereddine, B. Pakhaliuk, O. Husev and R. M. Strzelecki, "Power Converter Solutions for Industrial PV Applications—A Review," in Energies, vol. 15, p. 3295, 2022, doi: 10.3390/en15093295.	Journal	Published	10.3390/en15093295
2	M. Lukianov, I. Verbytskyi, N. Strzelecka and R. Strzelecki, "Power converter interface for urban DC traction substations - solutions and functionality," in Przegląd Elektrotechniczny, 2023, pp. 134–140, doi: 10.15199/48.2023.11.23.	Journal	Published	10.15199/48.2023.11.23
3	K. Nassereddine, M. Turzyński, M. Lukianov and N. Strzelecka, "Key activities to improve energy management in DC microgrids connected by urban traction," in Przegląd Elektrotechniczny, pp. 1–6, 2023, doi: 10.15199/48.2023.12.01.	Journal	Published	10.15199/48.2023.12.01
4	G. Arena, A. Chub, M. Lukianov, R. Strzelecki, D. Vinnikov and G. De Carne, "A Comprehensive Review on DC Fast Charging Stations for Electric Vehicles: Standards, Power Conversion Technologies, Architectures, Energy Management, and Cybersecurity," in IEEE Open Journal of Power Electronics, vol. 5, pp. 1573-1611, 2024, doi: 10.1109/OJPEL.2024.3466936.	Journal	Published	10.1109/OJPEL.2024.3466936
5	M. Lukianov, E. Romero-Cadaval, A. Kasprowicz, O. Husev and R. Strzelecki, "Scalable Multiport DC-DC Converter for Bidirectional EV Charging in DC Traction Grids," in IEEE Transactions on Circuits and	Journal	Published	10.1109/TCSII.2025.3572290

	Systems II: Express Briefs, vol. 72, no. 7, pp. 968-972, July 2025, doi: 10.1109/TCSII.2025.3572290.			
6	I. Verbytskyi, M. Lukianov, M. Bartłomiejczyk, S. Denysiuk and R. Strzelecki, "DC Traction Grids: Modernization Opportunities for Improving Efficiency and Profitability", Scientific Reports	Journal	Submitted	
7	Lukianov, M., Verbitsky, I., Cadaval, E.R., Strzelecki, R. (2024). An Overview of Bidirectional EV Chargers: Empowering Traction Grid-Powered Chargers. In: Kyrylenko, O., Denysiuk, S., Strzelecki, R., Blinov, I., Zaitsev, I., Zaporozhets, A. (eds) Power Systems Research and Operation. Studies in Systems, Decision and Control, vol 512. Springer, Cham. https://doi.org/10.1007/978-3-031-44772-3_9	Book Chapter	Published	10.1007/978-3-031-44772-3_9
8	I. Verbytskyi, M. Lukianov and R. Strzelecki, "Feature of Solar Radiation Forecast Services Use for Solar Plants," 2022 IEEE 8th International Conference on Energy Smart Systems (ESS), Kyiv, Ukraine, 2022, pp. 108-111, doi: 10.1109/ESS57819.2022.9969258.	Conference	Published	10.1109/ESS57819.2022.9969258
9	M. Lukianov, I. Verbytskyi, E. R. Cadaval and R. Strzelecki, "Bidirectional EV charger integration into LV DC traction grid," 2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Tallinn, Estonia, 2023, pp. 1-8, doi: 10.1109/CPE-POWERENG58103.2023.10227489.	Conference	Published	10.1109/CPE-POWERENG58103.2023.10227489
10	M. Lukianov, E. R. Cadaval, G. Arena and R. Strzelecki, "Partially Isolated Multi-Active Bridge DC-DC Converter with Bidirectional EV Charging Ports," 2024 IEEE 18th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Gdynia, Poland, 2024, pp. 1-7, doi: 10.1109/CPE-POWERENG60842.2024.10604312.	Conference	Published	10.1109/CPE-POWERENG60842.2024.10604312
11	K. Nassereddine, M. Turzyński, M. Lukianov and R. Strzelecki, "Advancing Solar Energy: Machine Learning Approaches for Predicting Photovoltaic Power Output," 2024 IEEE 18th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Gdynia, Poland, 2024,	Conference	Published	10.1109/CPE-POWERENG60842.2024.10604373

	pp. 1-6, doi: 10.1109/CPE-POWERENG60842.2024.10604373.			
12	M. Lukianov, P. Derkacz and R. Strzelecki, "Multi Active Bridge converter with DPS modulation for bidirectional EV charging from DC traction grid," IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024, pp. 1-7, doi: 10.1109/IECON55916.2024.10905342.	Conference	Published	10.1109/IECON55916.2024.10905342
13	M. Lukianov, E. R. Cadaval, O. Matiushkin and R. Strzelecki, "Traction powered multiport DC-DC converter for bidirectional EV charging application – HIL simulation results," 2025 IEEE 19th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Antalya, Turkiye, 2025, pp. 1-6, doi: 10.1109/CPE-POWERENG63314.2025.11027251.	Conference	Published	10.1109/CPE-POWERENG63314.2025.11027251
14	M. Lukianov, E. R. Cadaval, O. Matiushkin and R. Strzelecki, "Multi-terminal EV fast charging station based on multiport CF-MAB converter" 2026 IEEE 20th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)	Conference	Submitted	

Patents

#	Title	Type (National-Country, International-Scope)	Status (Submitted, published)	REFERENCE
1	R. Strzelecki, M. Lukianov, "Układ wielostanowiskowy stacji ładowania pojazdów elektrycznych" [Multi-port electric vehicle charging station], Poland Patent P.448300, April 15, 2024.	National-Country	Submitted	https://ewyszukiwarka.pue.uprp.gov.pl/search/pwp-details/P.448300

3.3. Task 3.3 – IRP7 "Reliability and Availability of Smart Transformers for Cost Effective and High Quality of Services in the Grid"

3.3.1. Introduction

This IRP focuses on the smart transformer (ST), a power-electronics-based transformer that can connect medium-voltage and low-voltage (MV and LV) AC and DC grids. In the first stage of the project, various ST architectures were studied in detail, and the potential use of the Modular Multilevel Converter (MMC) in AC/DC hybrid grids and STs was investigated. In the three-stage ST architecture shown in Fig. 1, MMC was identified as a promising solution for the MV AC-DC conversion stage because of its high modularity, scalability, and controllability. It can operate in the MV voltage range using low-voltage switches and can form an MV DC link without the need for a bulky capacitor.

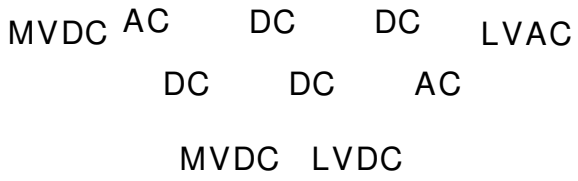


Fig. 1. Three-stage smart transformer (ST).

This research started with an investigation of the role of the MMC in different solid-state transformer architectures and inside the hybrid AC-DC grids. It then progressed to the modification of the sorting-based voltage balancing method by including switch junction temperature and capacitor losses in the balancing process. In the new developed voltage balancing method, decision factor is based on estimated junction temperature, calculated capacitor losses, and measured capacitor voltages with the goal of balancing all these parameters.

The next part of the research addressed the fault-tolerant operation of the converter through the use of redundant submodules, where both hot (active) and cold (passive) redundancy were studied. The results were presented for the hybrid MMC, which is composed of both FB and HB submodules. The operation of the hybrid MMC with hot reserve submodules was investigated. For cold reserve submodules, a new insertion method was proposed to suppress the high inrush current at the moment of insertion.

Finally, a test bench referred to as the MMC emulator was introduced as a cost-effective and safe platform for testing MMC-related topics. In this approach, a virtual MMC model running on a real-time simulator is combined with an actual submodule to represent the behaviour of the complete converter. Furthermore, methods for implementing MMC models on the real-time simulator were studied, and suitable approaches were presented.

The investigated topics and the results and findings have been published in conference and journal papers. These scientific outcomes were achieved during a 36-month research period at the facilities of the Chair of Power Electronics at Kiel University (Christian-Albrechts-Universität zu Kiel).

3.3.2.Scientific outcomes

3.3.2.1. Hybrid Modular Multilevel Converter

The Modular Multilevel Converter (MMC) is a modular converter composed of cascaded submodules (SMs). The series connection of the submodules and an inductor, called the arm inductor L_{arm}, forms an arm. Each phase of the MMC consists of two arms, namely the upper arm and the lower arm. The topology of the MMC is illustrated in Fig. 2, where R_{arm} denotes the equivalent arm resistance. The full-bridge (FB) and half-bridge (HB) submodules are among the most common SM structures in MMCs, depicted in Fig. 2(d) and Fig. 2(d). A bypass mechanism is added at the ac terminals of the SMs so that a faulty SM can be bypassed when a SM failure happens. This mechanism is an important part of the SMs and has a key role after fault detection in the converter.

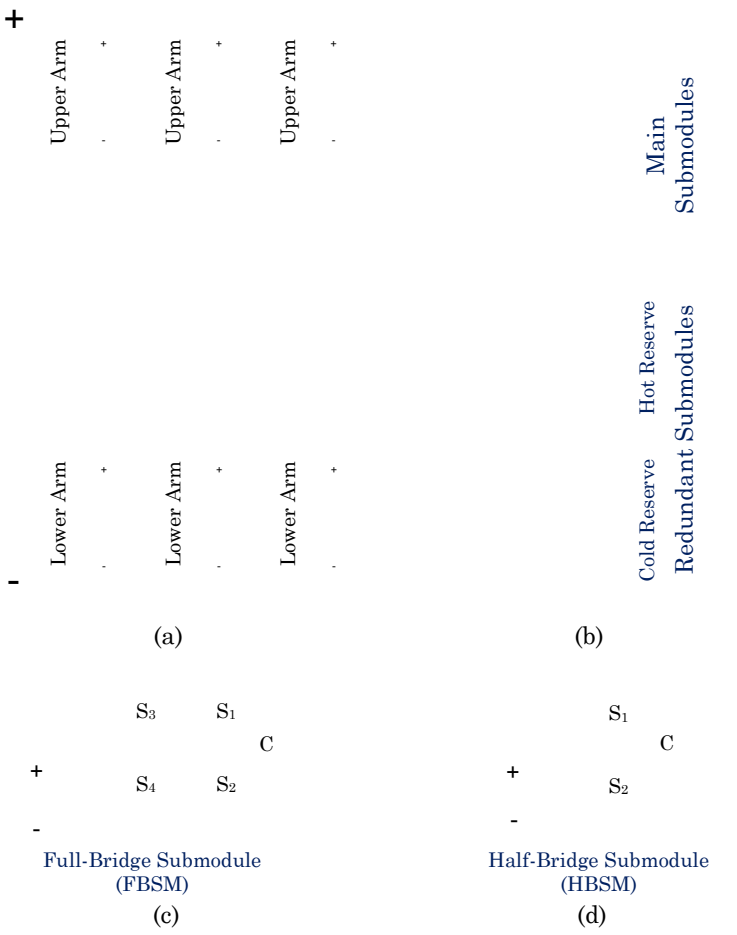


Fig. 2. Modular multilevel converter, (a) generic structure of MMC, (b) one phase of MMC consisting hot and cold reserve SMs, (c) full-bridge, and (d) half-bridge SM.

The HB SM has become the dominant option because of its cost-effectiveness and lower losses. However, the use of HB SMs in the MMC makes the converter unable to block DC fault current, which is a critical issue in applications such as fast-charging stations, DC transmission lines, and smart transformers. To address this limitation, FB SMs can be used instead.

In addition, the use of full-bridge (FB) SMs enables the MMC to operate in the overmodulation region. As a result, the converter can operate with a higher AC-side voltage or a lower DC-link voltage while maintaining the desired AC-side voltage. It has been shown in the literature that the use of FB submodules in the MMC provides a wide range of benefits. However, complete replacement of HB SMs with FB SMs results in higher losses and increased investment cost. To reduce these additional losses and costs, a hybrid MMC (H-MMC), consisting of both HB and FB SMs, can be employed instead of fully replacing the HB SMs. The H-MMC can partially provide the mentioned benefits, such as DC fault current blocking and operation under overmodulation conditions, while keeping the investment cost lower. The ratio between HB and FB SMs can be determined according to the application requirements and design considerations. As shown in Fig. 2 (b), redundant cold-reserve SMs are added to each arm. Therefore, the total number of SMs in each arm is given by (1).

$$N_{\mathrm{SM,total}} = N_{\mathrm{HB}} + N_{\mathrm{FB}} + N_{\mathrm{R,cold}} + N_{\mathrm{R,hot}} \quad (1)$$

Here, N_{HB}, N_{FB}, $N_{R,cold}$, and $N_{R,hot}$, represent the number of HB, FB, cold reserve, and hot reserve SMs, respectively. The total capacitor voltage in each arm is denoted by $V_{C,total}$ and is calculated as follows in (2). Note that the main objective of this report is to demonstrate the proposed method for the suppression of the inrush current during the cold reserve insertion. Therefore, the number of hot reserve SMs is assumed to be zero, $N_{R,hot} = 0$, in the rest of this document.

$$V_{\mathrm{C,total}} = (N_{\mathrm{HB}} + N_{\mathrm{FB}}) \times V_{\mathrm{C}} \quad (2)$$

where V_C is the voltage of one SM capacitor. If the capacitor voltages are balanced at V_C, the voltage of each arm can change within the maximum and minimum limits given in (3):

$$-N_{FB} \times V_C \leqslant v_{u,l,x} \leqslant V_{C,total} \tag{3}$$

where $v_{u,l,x}$ represents the arm voltage of the generic phase x ($x \in \{a,b,c\}$). The minimum arm voltage depends on N_{FB}. The ratio of N_{FB} to N_{HB} affects the ability of the H-MMC to work in overmodulation mode. This is achieved by controlling the dc and ac modulation indices, written as m_{dc} and m_{ac}. The relation between the dc-link voltage, V_{dc}, the ac-side voltage, and $V_{C,total}$ is given in (4):

$$m_{dc} = \frac{V_{dc}}{V_{C,total}} \tag{4}$$

$$m_{ac} = \frac{V_x}{V_{C,total}/2} \tag{5}$$

The values of N_{FB} to N_{HB} can be selected based on the converter's operating range and the minimum required dc-link voltage in the H-MMC. Since the upper and lower arm voltages behave in a similar way, only the upper-arm voltage condition is considered here. If the voltage drops across L_{arm} and R_{arm} are ignored, and using (4) and(5), the minimum upper-arm voltage can be written as:

$$v_{u,min,x} = V_{C,total}\left(\frac{m_{dc}}{2} - \frac{m_{ac}}{2}\right) \tag{6}$$

When FB SMs are used, the minimum arm voltage is shifted from 0 to $N_{FB} \times V_C$. As a result, the following condition is obtained:

$$V_{C,total}\left(\frac{m_{dc}}{2} - \frac{m_{ac}}{2}\right) \geq -N_{FB} \times V_C \Rightarrow m_{dc} - m_{ac} \geq \frac{-2N_{FB}}{N_{SM}} \tag{7}$$

Here, N_{sm} is the number of active SMs, excluding the cold-reserve SMs. Another important condition for m_{dc} and m_{ac} is given in (8).

$$\left|\left(\frac{m_{dc}}{2} + \frac{m_{ac}}{2}\right)\right| \leq 1 \Rightarrow 2 \leq |m_{dc} + m_{ac}| \leq 2 \tag{8}$$

From conditions (7) and (8), it can be seen that the H-MMC allows control of both dc and ac modulation indices, and this capability is affected N_{FB}.

3.3.2.2. Control and Modulation of H-MMC

The primary objective of the H-MMC control system is to generate voltage references for each arm. This ensures the required ac- and dc-side voltages while simultaneously addressing internal control objectives, such as balancing the SM capacitor voltages and suppressing circulating currents. The resulting arm voltage reference is then sent to the modulation block, which decides how many SMs needs to be inserted, referred to as the insertion index, N_{ins}. The overall control structure is presented in Fig. 3(a). Figure 3(b) shows the current controller, which receives the i_d and i_q references from the outer controller and generates the three-phase voltage reference. In addition, Fig. 3(c) and Fig. 3(d) present the energy-balancing and circulating-current controllers for each phase, which generate v_{ebc} and v_{ccc}, respectively. These signals are then added to the arm voltages of each phase.

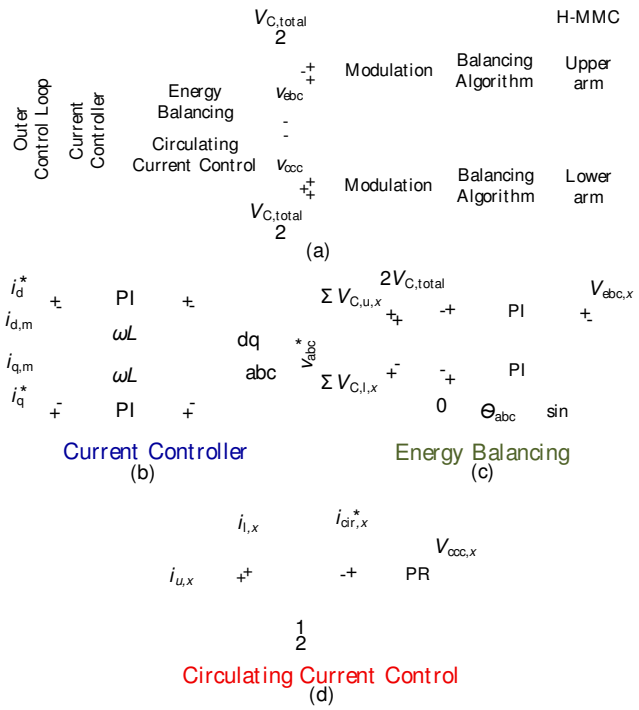


Fig. 3. Overall control scheme of the H-MMC, (a) current controller, (b) energy balancing, and (c) circulating current controller.

In this work, level-shift PWM (LS-PWM) is exploited to generate the arm insertion index N_{ins}. For SM voltage balancing in an H-MMC, the most commonly used approach is based on a sorting algorithm. The conventional voltage-balancing method is shown in Fig. 4. In this approach, when \(N_{\text{ins}}\) is positive, the inserted SMs are selected from the sorted list according to the direction of the arm current. If the arm current is negative, the SMs with the highest voltage values are inserted. Conversely, if the arm current is positive, the SMs with the lowest voltage values are inserted. When N_{ins} is negative, only the required full-bridge (FB) SMs are selected. In this case, for positive arm current, the FB SMs with the highest voltages are chosen, whereas for negative arm current, the FB SMs with the lowest capacitor voltages are inserted.

3.3.2.3. Proposed Cold Reserve SM Insertion Method

In Fig. 5, the overall structure of the proposed method is presented. The added blocks do not modify the existing control or modulation stages. Therefore, the modulation block can employ any modulation scheme, as its role in this architecture is limited to determining N_{ins}. The proposed method begins by ensuring that the voltage of the faulty SM is excluded from the converter control. Then, a parabolic charging profile is introduced and added on the measured voltage of the cold-reserve SM, enabling its insertion to be regulated through the coefficient of the parabolic function. Finally, these values are sent to the conventional sorting based voltage balancing algorithm, meaning that the main sorting algorithm remains unchanged. The following sections describe these steps in detail.

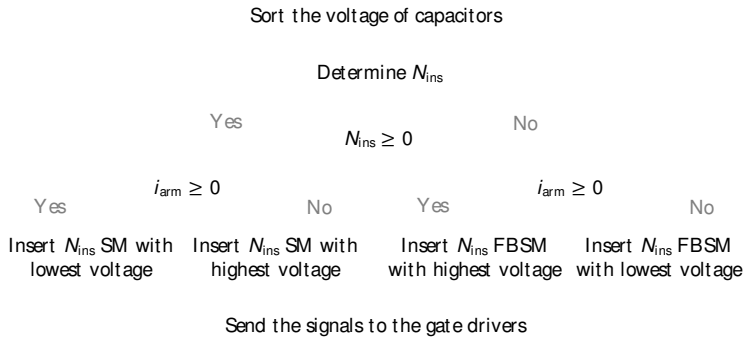


Fig. 4. Sorting-based capacitor Voltage balancing algorithm for H-MMC.

To prevent a faulty submodule (SM) from causing further disruption to converter operation, it must be rapidly detected and bypassed through a bypass switch. The fault detection unit identifies the faulty SM and typically bypasses it within a few fundamental cycles. Once the faulty SM is bypassed, the capacitor voltages of the remaining SMs increase, as described in (9).

$$\underbrace{\frac{V_{\mathrm{C,total}}}{N_{\mathrm{SM}}}}_{\text{pre-fault}} < \underbrace{\frac{V_{\mathrm{C,total}}}{N_{\mathrm{SM}} - N_{\mathrm{faulty}}}}_{\text{faulty}} \tag{9}$$

Here, N_{faulty} denotes the number of bypassed faulty SMs. The resulting increase in capacitor voltage may damage the capacitors and switching devices of the remaining healthy SMs. Since MV H-MMCs contain fewer SMs than HV H-MMCs, the voltage rise across the remaining healthy SMs becomes more noticeable. In addition, once a fault has been detected and the faulty SM has been bypassed, it is essential to remove both the affected SM and its associated measured voltage from the converter control system. If the faulty SM remains included in the control loop, the voltage-balancing algorithm may attempt to regulate its voltage together with those of the healthy SMs, leading to degrade the performance of the H-MMC.

The proposed method for excluding the faulty SM from the voltage balancing is illustrated in Fig. 5(a). In this approach, the actual voltage of the faulty SM during insertion and charging is replaced by a virtual value generated by the controller of the H-MMC, and this value is then provided to the sorting algorithm. To ensure proper operation, a value significantly higher than V_{C} is selected; for example, V_{fault} can be chosen as $2V_{\mathrm{C}}$. When i_{arm} and N_{ins} have the same sign, the algorithm replaces the faulty SM voltage, $v_{\mathrm{C,faulty}}$ with V_{fault} in the SM voltage-balancing algorithm. Conversely, when i_{arm} and N_{ins} have opposite signs, V_{fault} is set to zero. As a result, the faulty SM is never selected by the voltage-balancing process under any operating condition, without requiring any direct modification of the original voltage-balancing method.

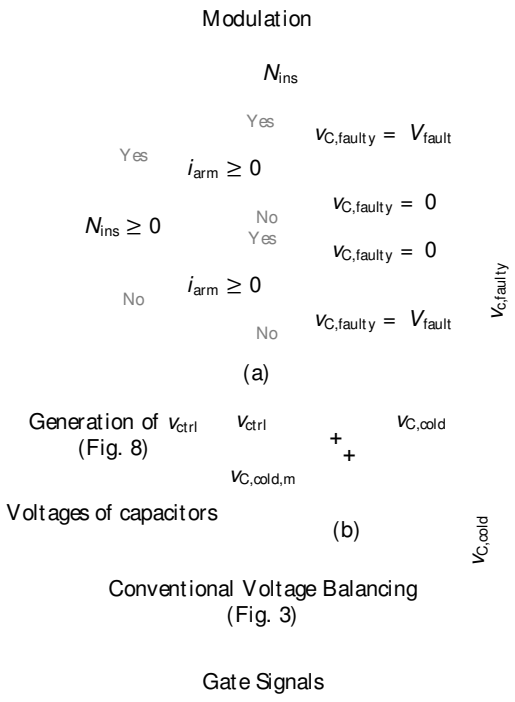


Fig. 5. Overall scheme of proposed method, (a) A function to disregard the faulty SM in voltage balancing, (b) integration of proposed method in sorting.

When a cold-reserve SM is inserted, its capacitor voltage initially exhibits the largest deviation from the nominal value, so it is exposed to the highest stress. If the cold-reserve SM is inserted without a dedicated control strategy, the newly added SM remains in charging mode and attempts to reach the nominal voltage as fast as possible. This results in a large current flowing through the SM. The capacitor current of the SM, i_{C}, depends on the arm current $i_{\mathrm{u,l}}$ and the switching function of the SM, S, as shown in (10):

$$i_{\mathrm{C}} = i_{\mathrm{u,l}} \times S \tag{10}$$

To avoid the problems associated with uncontrolled insertion and to regulate the current flowing through the SM, (10) indicates that either the arm current or the switching behaviour must be controlled. Since the arm current cannot be directly regulated for this purpose, the switching behaviour is controlled instead. If the cold-reserve SM can be controlled directly, its modulation reference, S_{ref}, is defined by a parabolic function. The general form of this function is given in (11) and illustrated in Fig. 6:

$$S_{\mathrm{ref}} = at^2 + bt + c \tag{11}$$

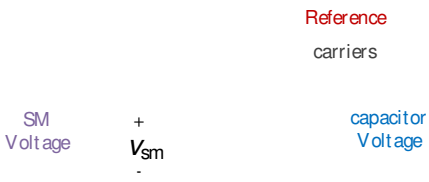


Fig. 6. Directly charging of the SM with the parabolic reference.

The parabolic function provides a smooth increase at the beginning of the charging process, which is particularly important during the insertion stage. If the switching frequency is sufficiently high, the capacitor current can be expressed in terms of this modulation reference, as shown in (12):

$$i_{\mathrm{C}} = i_{\mathrm{u,l}} \times S_{\mathrm{ref}} \tag{12}$$

The following discussion assumes that all SM capacitor voltages are balanced and that circulating currents are effectively suppressed. Under these conditions, the arm current in the H-MMC is given by (13):

$$i_{u,l} = \frac{I_{dc}}{3} \pm I_{ac}\sin(\omega t + \varphi) \tag{13}$$

where I_{dc} is the dc current and I_{ac} is the peak value of the ac-side current. By substituting (11) and (13) into (12), the following expression is obtained for the upper arm. Since the upper and lower arms exhibit similar behaviour, only the upper arm of phase "a" is considered.

$$i_C = at^2\frac{I_{dc}}{3} + bt\frac{I_{dc}}{3} + c\frac{I_{dc}}{3} + at^2 I_{ac}\sin(\omega t) + btI_{ac}\sin(\omega t) + cI_{ac}\sin(\omega t) \tag{14}$$

When the capacitor voltage is zero, the capacitor experiences the highest stress. To ensure that the charging process starts with zero slope, the derivative of the parabolic function is set to zero at the insertion instant. Therefore, the preferred value of b is zero. Choosing b = 0 also simplifies the function. In addition, since charging begins from zero, the parameter c should also be set to zero. As a result, (14) reduces to (15):

$$i_C = at^2\frac{I_{dc}}{3} + at^2 I_{ac}\sin(\omega t) \tag{15}$$

The effect of changing the parameter a is shown in Fig. 7. Based on (10), and assuming that S_{ref} follows the parabolic reference given in (11), the capacitor currents for six different values of a ($a_1 < a_2 < a_3 < a_4 < a_5 < a_6$) are presented in Fig. 7(a). It should be noted that these currents are obtained under the assumption that the SM produces a continuous waveform instead of a switching signal, with S_{ref} treated as a continuous function from (11). Using these current waveforms, the capacitor voltage is then calculated from (16) and shown in Fig. 7(b).

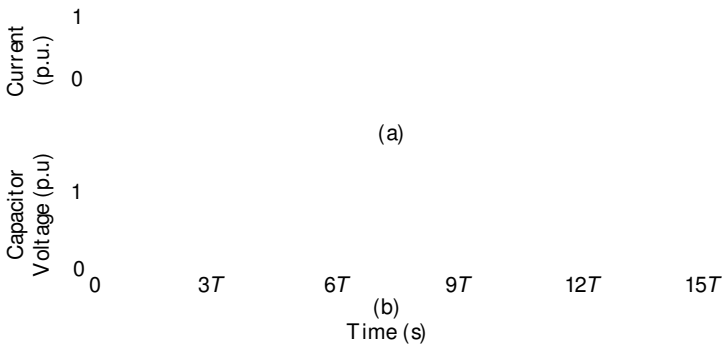


Fig. 7. Impact of changing parameter a in parabolic function on (a) capacitor current, and (b) capacitor voltage.

$$v_C(t) = \frac{1}{C}\int S_{ref} \times i_{arm}\mathrm{d}t \tag{16}$$

Controlling the switching behaviour also helps reduce the high RMS charging current, particularly during the initial stage of insertion. The RMS value of the capacitor current can be calculated as given in (17):

$$i_C^{rms} = \sqrt{\frac{1}{T}\int i_C{}^2 \mathrm{d}\,t} = \sqrt{\frac{1}{T}\int (i_{arm} \times S)^2 \mathrm{d}\,t} \tag{17}$$

Here, T is the fundamental period of the arm current. To clarify this concept, Fig. 8 shows the capacitor current of a general SM for different insertion periods within one cycle. By changing the SM switching pattern, the insertion period can be adjusted. Considering three different insertion periods per cycle, $T_{cap,1}$, $T_{cap,2}$, and $T_{cap,3}$, corresponding to Fig. 8(a)–(c), respectively. The insertion period in each cycle is defined as the sum of the time intervals during which the current flows through the capacitor, t_i, as given in (18):

$$T_{cap} = t_1 + t_2 + \cdots + t_i \qquad i\text{:Number}\sim\text{of}\sim\text{Switching} \tag{18}$$

By employing an appropriate control strategy, the switching commands can be adjusted to achieve a shorter insertion time. As a result, the capacitor is exposed to a smaller RMS arm current. In this example, $T_{cap,1} > T_{cap,2} > T_{cap,3}$, which means the waveform in Fig. 8(a) has the highest RMS current, while Fig. 8(c) has the lowest. Therefore, reducing the insertion period from $T_{cap,1}$ to $T_{cap,2}$ and then to $T_{cap,3}$ lowers the RMS capacitor current. Consequently, the high inrush current can be effectively mitigated by controlling the switching commands to limit the insertion period and by applying a regulated charging process to the cold-reserve SM, allowing its voltage to rise gradually to the nominal value.

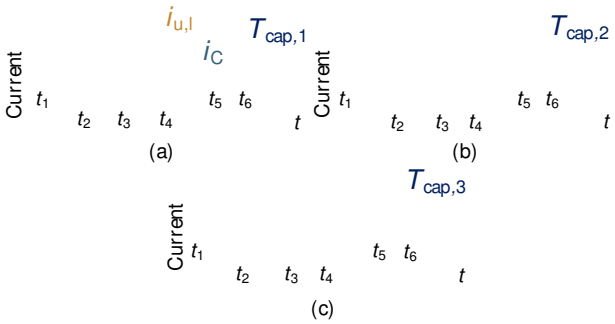


Fig. 8. Submodule capacitor current with different insertion times, (a) $T_{cap,1}$, (b) $T_{cap,2}$, and (c) $T_{cap,3}$.

As mentioned earlier, the switching behaviour of the SM cannot be controlled directly because it is determined by the voltage-balancing stage. The capacitor voltage-balancing stage generates the gate commands and balances the capacitor voltages based on N_{ins} and the measured capacitor voltages. After the cold-reserve SM is inserted, the voltage-balancing method generates its switching signal so that the SM capacitor charges toward its rated voltage and eventually becomes balanced with the other SMs. For a HB SM, this means that the capacitor is charged when the SM is inserted and the arm current is positive. For a cold-reserve FB SM, the capacitor is charged when the SM is inserted and the insertion index of the SM has the same sign as the arm current.

To prevent uncontrolled charging, the proposed method introduces a controlled value, v_{ctrl}, that temporarily represents the voltage of the cold-reserve SM. This value is gradually replaced by the actual measured voltage until the SM is fully charged. In this method, the voltage of the cold-reserve SM used by the voltage-balancing algorithm is the sum of v_{ctrl} and the measured voltage, as shown in (19) and Fig. 4(b):

$$v_{C,cold} = v_{C,cold,m} + v_{ctrl} \tag{19}$$

The value of $v_{C,cold}$ from (19) is then used in the voltage-balancing process. To regulate v_{ctrl}, a parabolic function with the general form given in (20) is used:

$$v_{ctrl} = -at^2 + bt + c \tag{20}$$

In this way, by adjusting v_{ctrl}, the capacitor voltage of the cold-reserve SM can be controlled. This method is illustrated in Fig. 9. The parabolic function provides a smooth slope at the beginning of the charging process, which is very important during insertion. For the reasons explained earlier, the selected value of b is zero. Also, the initial value of v_{ctrl} should be at least equal to the nominal capacitor voltage, V_C. In practice, this value is chosen slightly higher than the nominal value to account for capacitor voltage ripple, and it is set equal to the maximum measured capacitor voltage among all capacitors, $v_{C,max}$. Therefore, (21) can be written as:

$$v_{ctrl}(t) = -at^2 + v_{C,max}(t) \tag{21}$$

As time goes on, v_{ctrl} decreases, which causes the actual capacitor voltage to increase. The parameter a is constant and should be selected based on the maximum allowable current of the semiconductor devices and capacitors, as well as the desired charging time, t_{ins}. If all capacitor voltages are assumed to be properly balanced at their nominal value, then "a" can be calculated from (22):

$$a = \frac{V_C}{t_{ins}^2} \tag{22}$$

The charging time must be selected such that the inrush current remains within the allowable limit of the capacitor. Assuming that the charging process of the cold-reserve SM takes k_{ins} fundamental switching periods, the RMS capacitor current must always remain below its rated value to ensure that no harmful inrush current occurs. In other words, once the insertion time is chosen, the parameter "a" is determined accordingly. However, the selected insertion time, t_{ins}, must still be verified to ensure that it effectively limits the inrush current. With the proposed parabolic function, the capacitor voltage changes according to (23). In deriving this expression, $V_{C,max}$ is assumed to be constant and equal to the nominal voltage of the SM capacitors.

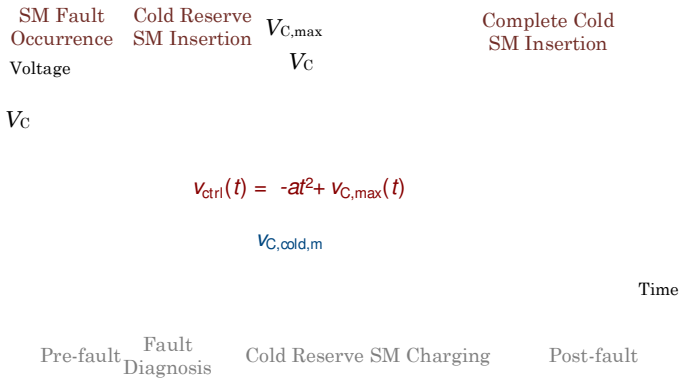


Fig. 9. Proposed cold reserve SM seamless charging method.

$$V_{C,cold} = at^2 \tag{23}$$

As a result, the capacitor current can be written as:

$$i_C(t) = C\frac{dv_C(t)}{dt} = 2aCt \tag{24}$$

By substituting (24) into (17), the RMS capacitor current is obtained as expressed in (25). Therefore, to validate the selected t_{ins}, the RMS capacitor current in each charging cycle must remain below the allowable rated capacitor current.

$$i_C^{RMS} = \frac{2aC}{\sqrt{T}}\sqrt{\int_{(k-1)T}^{kT} t^2 dt} \tag{25}$$

The calculated value of $i_C{}^{RMS}$ must stay below $i_{C,max}{}^{RMS}$ for (k = 1, 2, … , k_{ins}), where k_{ins} is the number of required cycles and is calculated as:

$$k_{ins} = \left\lceil \frac{t_{ins}}{T} \right\rceil \tag{26}$$

Therefore, the initial value of t_{ins}, which is chosen based on MMC parameters such as the SM capacitance, can be further checked and refined. In particular, if the RMS current for the selected t_{ins} is still higher than the target limit, the number of charging cycles should be increased, and the related equations should be recalculated until a suitable value of t_{ins} is found. This step-by-step process is important to make sure that the selected insertion time is effective in reducing the inrush current.

3.3.2.4. Simulation Results

This section presents MATLAB/Simulink simulation results to demonstrate the feasibility and effectiveness of the proposed method. A three-phase MMC with 12 SMs and one cold-reserve SM in each arm is considered. Although the proposed method can regulate the charging of the cold-reserve SM for both HB and FB SM configurations, the FB cold-reserve SM is preferred. Employing an FB SM as the cold reserve ensures that, following a fault, the ratio N_{FB}/N_{SM} does not decrease. As a result, the converter retains its capability to operate under overmodulation conditions. The remaining simulation parameters are listed in Table I. In all simulation cases, a duration of 50 ms is assumed for fault detection, fault localization, and control system response. This interval may vary depending on several factors, such as the type of SM fault and the fault diagnosis method employed. During this period, the arm current becomes distorted.

Table I. Simulation and Experimental Parameters

Specifications	Simulation	Experiment
Number of HB SM per arm (N_{HB})	6	3
Number of FB SM per arm (N_{FB})	6	3
Number of Reserve SM per arm (N_R)	1	1
Voltage of capacitors (V_C)	4000 V	300 V
Capacitance of SMs (C_{SM})	2000 uF	940 uF
Arm inductor (L_{arm})	10 mH	6 mH
Arm equivalent resistance (R_{arm})	0.18 Ω	0.01 Ω
Switching frequency	2 kHz	2 kHz
Load resistor	25 Ω	50 Ω
Load inductor	20 mH	39 mH
Inductor in test bench	-	20 mH
Resistor in test bench	-	4 Ω
Test bench voltage source (V_S)	-	450 V

First, the uncontrolled charging of the cold-reserve SM is examined with a dc-link voltage of 48 kV and $m_{dc} = 1$. Figure 10(a)–(d) shows the simulation results for the pre-fault condition, fault period, insertion period, and post-fault operation when the cold-reserve FB SM is charged without control. During the fault condition, the arm voltage cannot properly produce the thirteen-level waveform, and the arm currents become distorted, as shown in Fig. 10(b). While the faulty SM is bypassed, the capacitor voltages of the remaining SMs increase according to (9), as shown in Fig. 10(c). Since the SM voltages are well balanced, Fig. 10(c) shows only one HB SM capacitor voltage and one FB SM capacitor voltage. The results show that the RMS current of the cold-reserve SM reaches 375 A, while its steady-state value is about 166 A. This means the RMS current increases by more than 125%. Figure 11 shows the uncontrolled charging of the cold-reserve SM during overmodulation operation $m_{dc} < 1$, with the dc-link voltage set to 38 kV. The MMC electrical variables for the pre-fault, fault, insertion, and post-fault operating conditions are shown in Fig. 11(a)–(d). In this case, the steady-state current is 197 A and the inrush current is 301 A. Therefore, the capacitor current increases by 57%. Under this operating condition, the HB and FB capacitor voltages have different waveforms. The capacitor voltages of SM number three (HB SM) and SM number ten (FB SM), along with the capacitor voltages of the faulty SM and the cold-reserve SM, are shown in Fig. 11(c). Because of the different m_{dc}, the capacitor current of the cold-reserve SM in Fig. 11(d) behaves differently from that shown in Fig. 10(d).

The inrush current mainly depends on the duty cycle of the cold-reserve SM during the insertion period. The capacitance of the SM capacitors, C_{SM}, does not directly affect the peak inrush current. However, C_{SM} does affect the arm current and the related distortion during the fault condition and diagnosis period, and therefore it indirectly influences the inrush current. This effect is illustrated in Fig. 12(a), in which changing C_{SM} affects the minimum charging time required. This relationship is shown in Fig. 12(b).

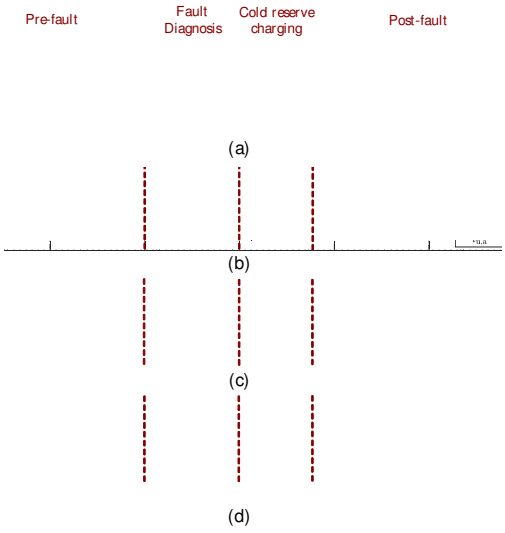


Fig. 10. Uncontrolled cold reserve SM charging with rated dc-link voltage m_{dc}=1, (a) upper and lower arm voltages, (b) upper and lower arm current, (c) capacitor voltages, and (d) capacitor current.

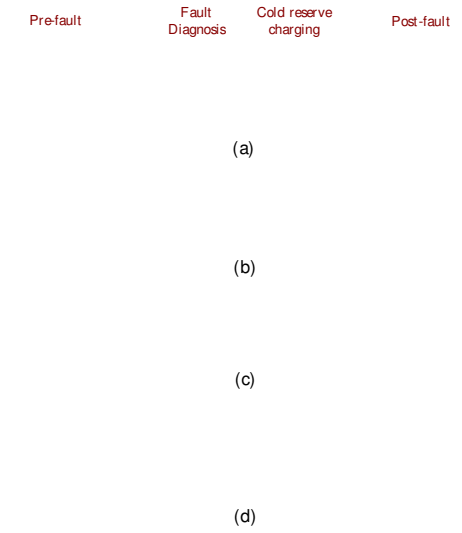


Fig. 11. Uncontrolled cold reserve SM charging with rated dc-link voltage m_{dc}<1, (a) upper and lower arm voltages, (b) upper and lower arm current, (c) capacitor voltages, and (d) capacitor current.

The performance of the proposed method for inserting the cold-reserve SM is evaluated through a detailed simulation, using the parameters listed in Table I. A fault occurs in the SM at t = 0.1 s, and the insertion of the cold-reserve SM starts at t = 0.15 s. The insertion period is set to 300 ms.

The results shown in Fig. 13, Fig. 14, and Fig. 15 present the complete operating sequence of the converter, including the pre-fault, fault, charging, and post-fault stages when the proposed charging method is used. The operation of both FB and HB SMs as cold-

Fig. 12. Dependency of the minimum charging time on the C_{SM} under uncontrolled charging conditions, (a) RMS of capacitor current, and (b) Cold reserve SM capacitor voltage.

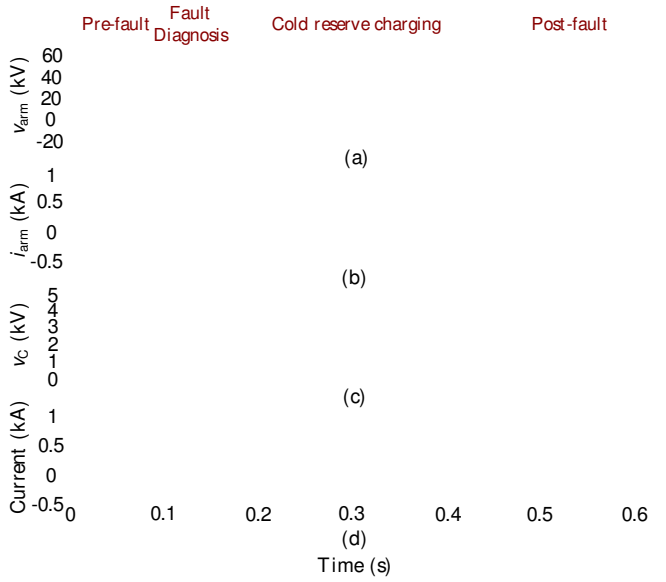


Fig. 13. Controlled charging of cold reserve SM by proposed method with m_{dc}=1, (a) upper and lower arm voltages, (b) upper and lower arm current, (c) capacitor voltages, and (d) capacitor current.

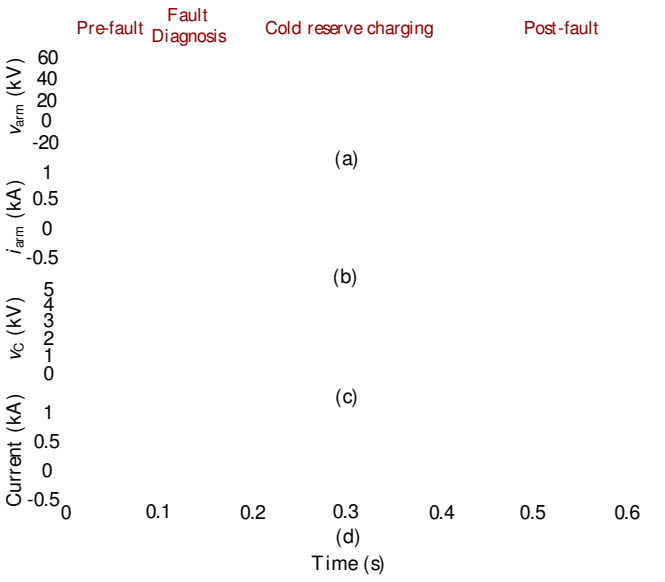


Fig. 14. Controlled charging of cold reserve SM by proposed method with m_{dc}<1, (a) upper and lower arm voltages, (b) upper and lower arm current, (c) capacitor voltages, and (d) capacitor current.

reserve SMs has been studied, and the results show that the proposed method can effectively control the charging of the cold-reserve SM regardless of the SM type.

Under operating conditions without overmodulation, all SMs produce only 0 and $+V_C$. As a result, the same charging profile and similar behaviour are observed for both HB and FB SMs when they are used as cold reserves. Figure 13(a) and Fig. 13(b) show the upper and lower arm voltages and currents. At the beginning of the insertion process, the upper-arm voltage and current are not generated properly and become distorted during the fault diagnosis and insertion period. However, as the cold-reserve SM voltage approaches its desired value, both the arm voltage and current improve and become more symmetrical.

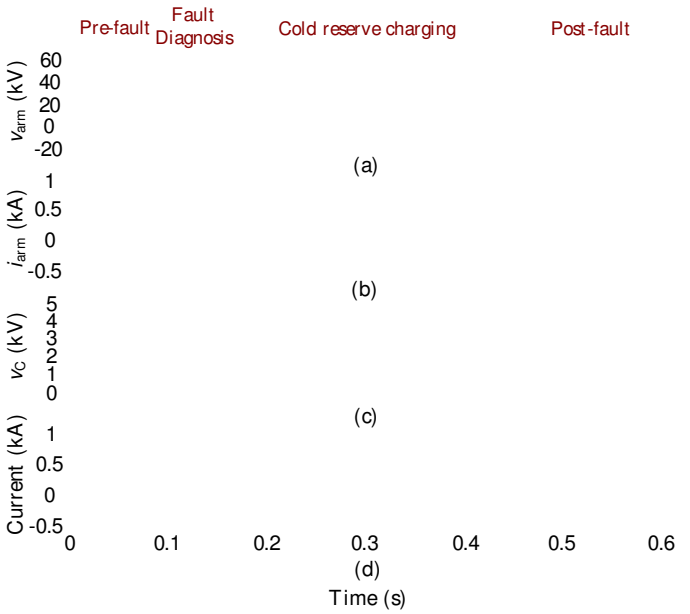


Fig. 15. Controlled charging of HB cold reserve SM by proposed method during overmodulation m_{dc}<1, (a) upper and lower arm voltages, (b) upper and lower arm current, (c) capacitor voltages, and (d) capacitor current.

The SM capacitor voltages are shown in Fig. 13(c). As can be seen, the voltage of the cold-reserve SM follows a parabolic shape during charging, which allows the SM to charge smoothly without sudden changes in voltage (dv/dt) or current (di/dt) in the capacitor. Figure 13(d) shows that the SM insertion duty cycle begins at a very low value and then increases gradually. The proposed method completely removes the inrush current.

In the same way, the effectiveness of the proposed method for the H-MMC under a lower dc modulation index m_{dc} < 1 and overmodulation conditions is shown in Fig. 14 and Fig. 15, where the cold-reserve SMs are FB and HB types, respectively. In this case, V_{dc} = 38 kV, and the FB SMs also generate negative voltage, which causes the capacitor voltages of the FB and HB SMs to have different waveforms. When the cold-reserve SM is an HB SM, its charging profile is different from that of the FB SM, as shown in Fig. 15(c). Hence, as explained before, the proposed method provides the same insertion time and ensures controlled operation for both SM types.

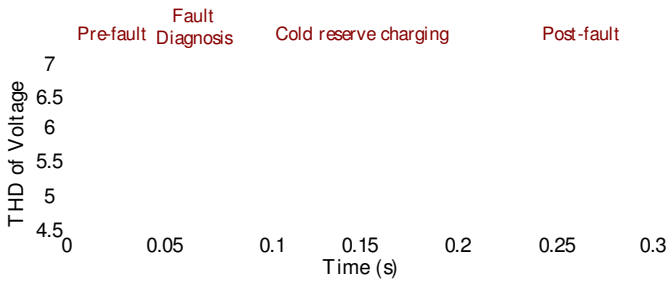
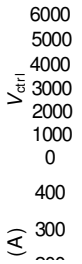


Fig. 16. THD of the output voltage for the faulty phase of the H-MMC during pre-fault, faulty, charging, and post-fault operation.

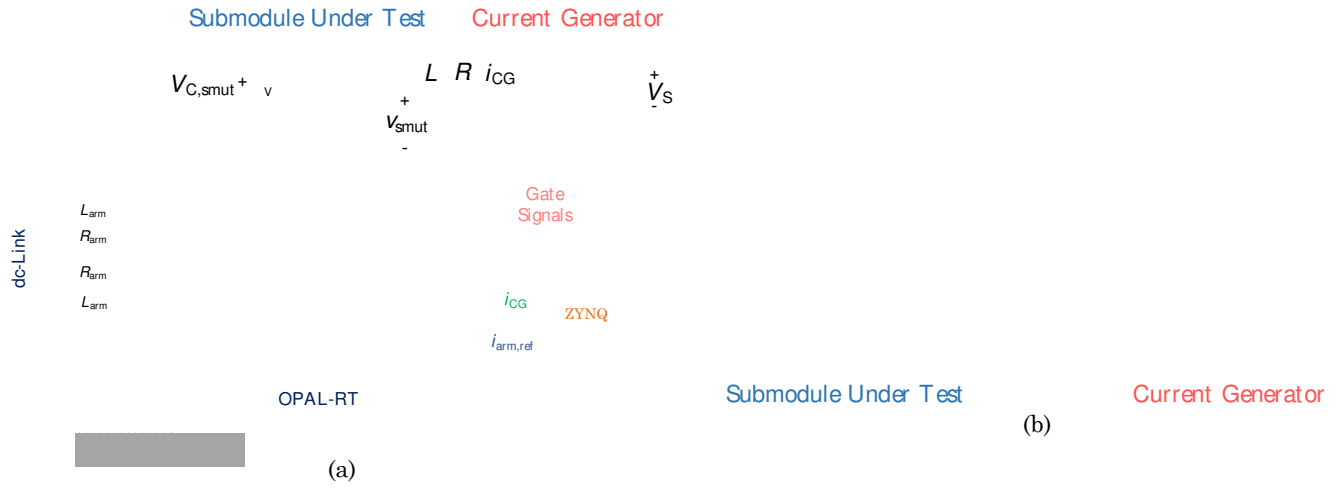
In addition, to evaluate how the proposed method affects the H-MMC voltage, the THD of the faulty phase output voltage is measured during each stage of operation, including pre-fault, fault, charging, and post-fault conditions, for every fundamental cycle. The results are shown in Fig. 16. In this test case, the THD increases from 4.9% to 6.3% in the worst case.

Different insertion times t_{ins} produce different levels of inrush current. To demonstrate this, several values of t_{ins} are used for cold-reserve insertion in Fig. 17. Figure 17(a) shows different values of V_{ctrl}, and the related inrush currents for each case are shown in Fig. 17(b). In addition, the results are summarized in Table II, where both the absolute values and the percentage increases relative to the steady-state current are reported.



(a)

3.3.2.5. Experimental Results



(a) (b)

Fig. 18. Experimental Setup: (a) concept of the experimental test bench, (b) actual experimental test bench.

To verify the feasibility and effectiveness of the proposed cold-reserve insertion method, a setup combining a real-time H-MMC model and an actual SM is used. This test bench is named as MMC emulator Since building a complete MMC system and the related test facility for experimental validation is expensive and time-consuming. A full MMC for high-power applications may contain tens to hundreds of SMs per arm, operating at kilovolt-level DC bus voltages

and megawatt-level power ratings. Even with the scaled-down prototype, testing scenarios involving manually applied faults or severe converter transients requires considerable additional effort. Furthermore, such conditions increase the experimental risk and may expose the converter to highly critical operating conditions. Using MMC emulator provides a practical way to avoid the high cost, large size, and design complexity usually associated with MMC systems. MMC emulator also provides an opportunity for industrial and research groups to accelerate the testing and validation of newly developed ideas and to facilitate the rapid development of MMC.

With the help of the actual SM exploited in this test bench, the electromagnetic and electrothermal behaviour of the SM can be tested by considering the operating characteristics of the MMC, such as the arm current, capacitor voltage fluctuations, and switching.

The general idea and structure of the test bench are shown in Fig. 18(a), while Fig. 18(b) presents the experimental setup. The test bench includes a real MMC cold-reserve SM, labeled in Fig. 18(b) as the SM under test (SMUT), a current generator based on an FB converter, and a real-time simulator. In this setup, the SMUT is connected to the H-MMC model running online on the OPAL-RT OP5700 FPGA-based real-time simulator.

To achieve high accuracy and fidelity, the H-MMC switching model is implemented on the electric hardware solver (eHS), an FPGA-based toolbox, with a sampling time of 800 ns. This FPGA-based implementation enables the switching behaviour of the H-MMC and its semiconductor devices to be captured with high accuracy in real time. As a result, the modelled converter can be operated using actual control and switching commands running in real time.

All the controllers, SMs and electrical components are included in the real-time model, implemented on the CPU with a sampling time of 25 µs, except the cold-reserve SM. This SM is replaced by a controlled voltage source driven by the actual and real-time measurement of the SMUT ac terminal voltage, v_{smut}.

The SMUT is charged through a current generator that follows the arm-current reference produced by the H-MMC model. The current generator is an FB converter controlled by a PR-based current controller implemented on a ZYNQ-7000 ARM/FPGA SoC. This separate device is used to avoid adding extra computational load to the real time simulator and to provide greater flexibility and controllability, which allows operation at higher frequencies and improves performance.

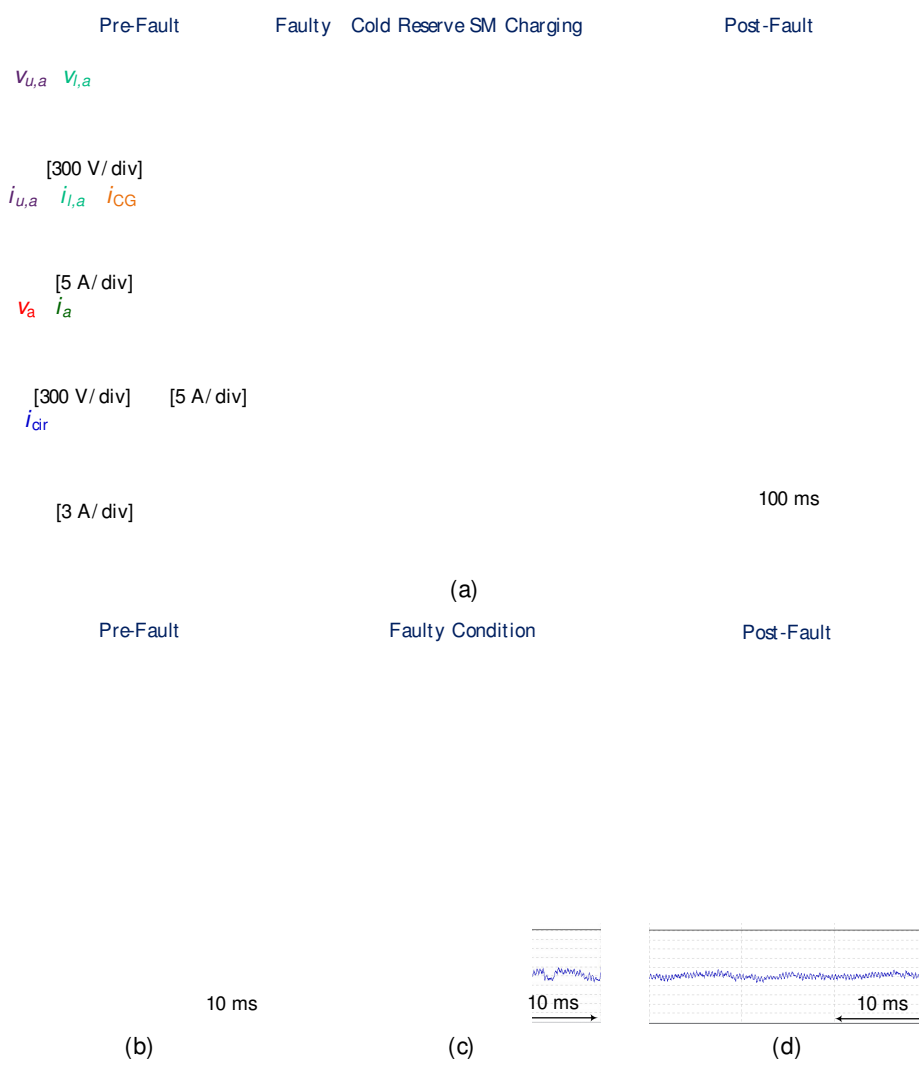


Fig. 19. Experimental results during pre-fault, faulty, charging phase of cold reserve SM, and post-fault operation conditions: (a) Overview of results, (b) zoomed view of pre-fault condition, (c) zoomed view of faulty condition, and (d) zoomed view of post-fault condition.

Gate signals for the SMUT are generated by the modulation strategy and voltage-balancing control running in the real-time simulator. Therefore, the SMUT capacitor voltage, $V_{C,smut}$, is measured and fed back to the real-time H-MMC model to support the sorting process, voltage balancing, and gate-signal generation. As a result, the SMUT behaviour, including its capacitor-voltage dynamics and ac-terminal voltage, closely matches that of an SM in a complete H-MMC setup. This approach makes it possible to study both the transient and steady-state performance of a full-scale converter effectively

In each arm of the H-MMC, three HB SMs, three FB SMs, and one redundant SM are used. The capacitance of all SMs, C_{SM}, is 940 µF, while the arm inductor L_{arm} and equivalent arm resistance R_{arm} are 6 mH and 0.1 Ω, respectively. The full experimental parameters are listed in Table I. The gate signals for the power devices are generated using LS-PWM with a switching frequency of 2 kHz.

The experimental validation results are shown in Fig. 19(a), where the arm voltages $v_{u,a}$, $v_{l,a}$, arm currents $i_{u,a}$, $i_{l,a}$, output voltage and current, v_a, i_a, and circulating current are presented under different operating conditions.

In this case study, the charging time is set to 300 ms. As shown, before the cold-reserve SM is fully inserted, the arm voltages and currents are distorted, and this distortion also appears in the output voltage. Zoomed-in views of these waveforms during the pre-fault, fault, and post-fault operation of the converter are provided in Fig. 19(b)–(d), respectively.

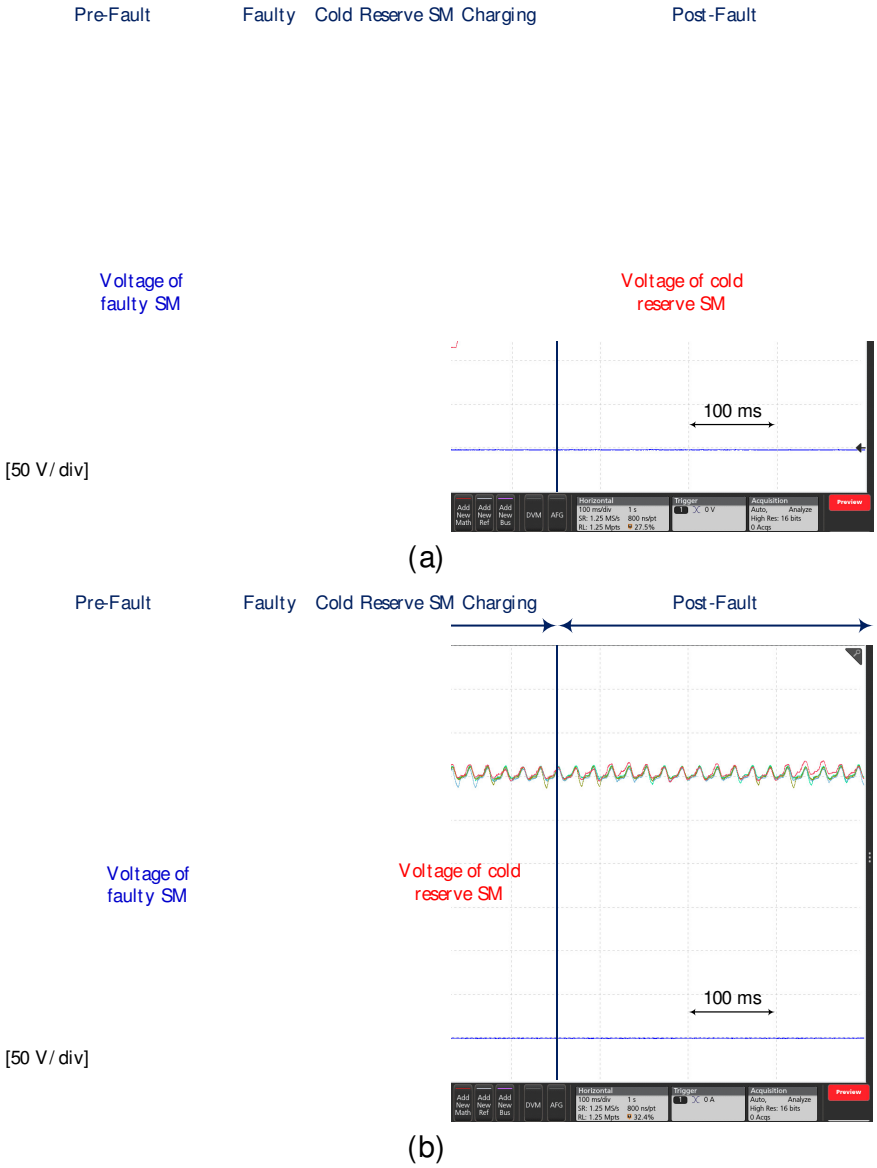


Fig. 20. Capacitor voltages, (a) proposed cold reserve SM insertion method, and (b) uncontrolled charging of cold reserve SM.

Figure 20 shows the capacitor voltages for both the proposed charging method and the uncontrolled charging method. To perform this comparison, one SM in the model is bypassed, and then the SMUT is inserted as a cold-reserve SM. In these two insertion methods, the capacitor currents are different, as illustrated in Fig. 21(a)–(f).

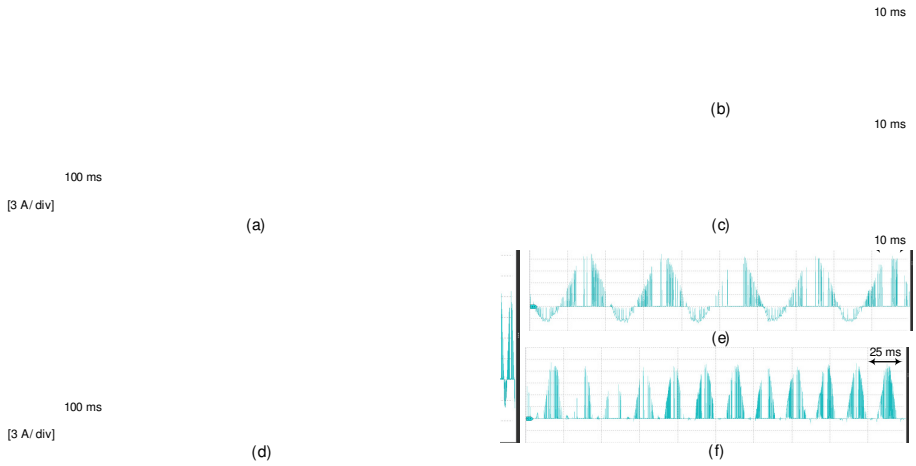


Fig. 21. Cold reserve SM capacitor current, (a) Uncontrolled cold reserve insertion, (b) zoomed-in view during the first few cycles of uncontrolled insertion, (c) zoomed-in view in the steady-state after uncontrolled insertion, (d) proposed cold reserve insertion method, (e) zoomed-in view during the first few cycles of proposed insertion method, (f) zoomed-in view in the steady-state by insertion of cold reserve SM with proposed method.

If the capacitor is inserted without control, as in Fig. 21(a), the duty cycle becomes very high, and as a result, both the peak and RMS capacitor current are also high. In contrast, with the proposed method, the number of switching actions and the duty cycle of the cold-reserve SM increase gradually, which makes it possible to limit the current. Zoomed-in views are also provided to show the difference between the two methods more clearly.

This difference is further shown in Fig. 22, where the uncontrolled charging case produces an RMS capacitor current nearly 149% higher than the rated value. In comparison, the proposed method effectively suppresses the excessive peak and RMS capacitor current.

Fig. 22. Comparison of the RMS values of the inrush current obtained from the proposed charging method and uncontrolled insertion.

3.3.3. Contribution to the WP objectives

The research conducted under IRP7 delivered several key outcomes related to the reliability and availability of smart transformers based on the Modular Multilevel Converter (MMC):

The conventional sorting-based capacitor voltage balancing algorithm was extended to incorporate switch junction temperature estimation and capacitor losses. This multi-objective balancing approach improves lifetime and thermal stress distribution across submodules, directly enhancing converter reliability. (Reported on the 1st annual report)

A cost-effective hardware-in-the-loop platform was developed, combining an FPGA-based real-time H-MMC model with a physical submodule and a ZYNQ-7000-controlled current generator. This platform enables safe and scalable testing of MMC fault-tolerance strategies without building a full-scale converter.

A new parabolic function based cold reserve charging strategy was developed for inserting submodules after a fault. The method:

- Excludes the faulty SM from the voltage-balancing loop by assigning a virtual voltage value.
- Introduces a controlled value added to the measured cold-reserve SM voltage, enabling the conventional sorting algorithm to gradually increase the SM's duty cycle.
- Uses a parabolic profile to ensure slow start, eliminating inrush currents.
- Simulation results demonstrated that uncontrolled insertion causes RMS capacitor current increases of 57–125% above steady-state values, while the proposed method completely removes the inrush current.

- Experimental validation on an MMC emulator test bench (OPAL-RT OP5700 + physical SMUT) confirmed that uncontrolled insertion produces 149% excess RMS current, which the proposed method effectively suppresses.

3.3.4. Scientific achievements

Experimental prototypes

#	Name	Description	Status (designed, assembled, tested)	Photo
	MMC Emulator	MMC emulator combining an FPGA-based real-time H-MMC model with a physical submodule	Designed and tested	Included in the report

Publication

#	Title, incl. citation information	Type (Conference, journal, book chapter)	Status (Submitted, accepted, published)	DOI
1	Modular Multilevel Converters Enabling Multibus DC Distribution	Conference	published	10.1109/CPE-POWERENG58103.2023.10227452
2	Modified Sorting Algorithm for Fault-Tolerant Operation of Hybrid MMC With Hot Reserve Submodules	Conference	published	10.1109/PEDG61800.2024.10667398
3	Fault Tolerant Control for Medium Voltage Hybrid MMC With Cold Reserve Submodules	Conference	published	10.1109/PEDG61800.2024.10667457
4	Arm Modeling Approaches for Real-Time Simulation of Modular Multilevel Converter	Conference	published	10.1109/PowerTech59965.2025.11180698
5	Arm Average Value Model of Hybrid MMC, Considering DC Fault and Internal Switch Failures	journal	published	10.1109/TIE.2025.3625285
6	Controlled Insertion of Cold Reserve Submodule in Hybrid Modular Multilevel Converter Considering Inrush Current Mitigation	journal	published	10.1109/TIE.2025.3647886
7	A Data-Driven Condition Monitoring Method for Capacitor in Modular Multilevel Converter (MMC)	Conference	published	10.1109/IPEMC-ECCEAsia60879.2024.10567101
8	Monolithic Data-Driven Condition Monitoring Strategy for MMC Considering *C* and ESR	journal	published	10.1109/TPEL.2025.3549226
9	Physics-informed neural network for parameter identification: A buck converter case study	Conference	published	10.1109/ECCE-Asia63110.2025.11111770
11	A Unified Framework for System-Level Condition Monitoring of Power Electronic Converters	journal	accepted	

3.4. Task 3.4 – IRP8 "Real-time modelling and validation of Distributed Energy Storage Systems and Integration strategies"

3.4.1. Introduction

The research activity associated with the ESR8 position has been carried out by two researchers: Gabriele Arena, from April 2022 to the end of 2024, and Danilo Di Berardino, who took over in April 2025. Although both phases share the same institutional setting — the Energy Lab 2.0 at the Institute for Technical Physics (ITEP), Karlsruhe Institute of Technology (KIT) — they differ in focus.

The first phase was conducted by Gabriele Arena. The research focused on DC networks, addressing several aspects: a comparison between isolated and non-isolated converter topologies in terms of efficiency and short-circuit behaviour; the modelling of a dual active bridge (DAB) converter through different integration techniques to assess their impact on the accuracy of power electronic simulations; and a comprehensive review of DC fast-charging stations, covering standards, isolation schemes, microgrid architectures, voltage and power levels, battery energy storage systems, and power converters. This theoretical groundwork was followed by an experimental phase, conducted from November 2023 to February 2024, in which experiments were carried out to verify the behaviour of the DAB converter over a wide output voltage range. Two conference publications supported this work, investigating the working principle of the DAB converter prior to the experimental campaign. As a final outcome, an experimental setup for flexible electric vehicle fast-charging stations was designed and assembled at KIT, targeting a reconfigurable 400V/800V system capable of achieving high efficiency across the full voltage range. Mr. Arena left the PhD programme at the end of 2024.

The second phase was taken over by Danilo Di Berardino, who joined in April 2025 with a partially modified research focus. Only a six-month portion of the full three-year research plan falls within the SmartGYsum doctoral programme, and the results presented here correspond to the first phase of a longer research agenda, conducted at the RTSET group within ITEP at KIT. Building on the DC network expertise developed in the first phase, the research shifts focus towards hydrogen-based energy systems, investigating the techno-economic feasibility of hydrogen-based energy storage (HES) integrated with photovoltaic (PV) generation in off-grid microgrids. This phase lays the economic and technical foundation for subsequent stages, which will include dynamic modelling in MATLAB/Simulink, development of control strategies, and experimental validation using the Power Hardware-in-the-Loop (PHIL) infrastructure of the H2-in-the-Loop (H2IL) facility at KIT Energy Lab 2.0. A dedicated MATLAB toolchain was developed to automate system sizing and economic assessment, designed to be replicable across different geographic locations and enabling a comparative feasibility assessment across diverse irradiance conditions in Europe.

3.4.2.Scientific outcomes (ESR08 - Gabriele Arena)

In former years environmental impact of fossil fuels brought to an increasing use of renewable energy resources (RES). However, directly connection of RESs and distributed generators (DGs) in general can bring to problems in terms of voltage deviation and protection issues, congestion of transmission lines and reduction of generators used to keep the desired grid frequency. In order to find a solution to these issues the concept of microgrid was invented. The increasing spread of power electronics in the electrical domain leads to consider DC for microgrids. In fact, DC microgrids have a series of advantages compared to AC microgrids. First of all, they have a less number of conversion stages, which makes them less complex and more efficient compared to AC microgrids. An AC microgrid does not require a rectification stage from the upper grid, but it needs an AC/DC conversion stage for every load and DG connected to it. On the other side, DC microgrids have an initial rectification stage from the upper grid but they do not require extra AC/DC conversion stages. Moreover, they are more suitable to interface DGs, such as photovoltaic panels, fuel cells, wind turbine and microgas turbines. DC microgrids do not even have any frequency issue and skin effects does not appear in DC, which allows to make the cables smaller and to reduce the costs. In order to prove the higher efficiency and reliability, the first experimental DC microgrid was developed by Ito et al. in 2004, with a power of 10 kW.

Despite these advantages, DC microgrids also present some challenges that researchers have been facing during the last years. The most important problem is related to the protections. In fact, whenever a fault occurs in DC microgrids, the fault current can reach up to 100 times the nominal current of the system in few milliseconds and protection devices cannot be developed based on the natural zero crossing point like in AC microgrids. For this reason, protection

devices are more complex and expensive in DC rather than in AC microgrids. A second problem is related to the transition from AC to DC infrastructure, which could take some years and large investments. Finally, power quality is another problem that must be faced in DC microgrids. Even though theoretically in DC there is no reactive power, the grid to which the DC microgrid is connected and the power converters inside the DC microgrid itself can introduce harmonic issues.

An example of DC microgrids is represented by telecom networks. Initially developed with a 48 V DC bus, research has investigated efficiency improvements through increasing the DC bus voltage up to 380 or 400 V. Other examples of DC microgrids are DC buildings and data centres, industrial and ship networks, more electric aircrafts, electrification of rural areas, and DC fast charging stations. In particular, research and development has grown in the last years in the area of DC fast charging stations. The reason behind this technology is the necessity to reduce the charging time of electric vehicles, making them comparable to combustion engine cars, in such a way to reduce the fear of costumers in the event of a long trip. For this reason, DC fast charging stations have been taken as test case of this research.

The following section covers DC fast charging stations, considering their standards, features, architecture, and power conversion technology. Then, a comparison between an isolated DC-DC converter, the dual active bridge (DAB), and non-isolated one, the four-switch buck-boost (FSBB) is presented. These two converters have been developed for an AC charging application, but they can be easily extended to DC fast charging. Finally, the modelling of a DAB converter has been reported since modelling is an important part of power electronic simulations. The modelling of such a converter has been taken under different integration methods to compare their accuracy and computational time.

DC Fast Charging of Electric Vehicles: Main Standards and Architectural Features

EV charging standards are different and have different classifications based on the country and/or continent. To simplify the explanation EV charging standards will be divided in AC charging standards and DC charging standards. Understanding the AC charging standards allows to understand the reason of the need of DC fast charging. To start with, the SAE J1172 standard is adopted in North America, Japan, and South Korea. It has two level of AC charging, respectively level 1, with a maximum charging power of 1.9 kW, and level 2, which a maximum charging power of 19.2 kW. IEC 61851 is instead the AC charging standard adopted in Europe. It is divided in 3 modes: mode 1 enables a maximum charging power of 13.3 kW, whereas mode 2 and 3 enables up top 22 kW of charging power. GB/T is the AC charging standard adopted in China and India, which provides up to 12.8 kW of charging power. The charging standard developed by Tesla and now open to all the other companies is known as north American charging standard (NACS) and it allows up to 11.5 kW of charging power.

It results clear that it is not possible to reach power ratings higher than 22 kW with AC charging. For this reason, DC charging is needed to provide charging power in the range of 50-400 kW. To start with, CHAdeMO provides is spread all over the world with a charging power of 400 kW. GB/T standard also offer DC fast charging with a maximum power transfer of 237.5 kW. CCS Type 1 is adopted in North America and South Korea and it offers a maximum power transfer of 350 kW. CCS Type 2 also offers a maximum power transfer of 350 kW but it is used in Europe and Australia. Finally, NACS is also adopted for DC charging and it reaches a maximum power of 350 kW . Furthermore, ChaoJi is a new standard resulting from the collaboration between the CHAdeMO association and the China Electricity Council. It is compatible with CHAdeMO, GB/T and maybe in future with CSS. It can reach a maximum charging power of 900 kW.

DC fast charging stations are typically connected into an AC microgrid, with a bus of 250-480 V line-to-line AC. This means that the MV uppergrid is connected to the AC microgrid with a MV/LV transformer. Such AC microgrid has the advantage to have well established technology, measurement and protection standards. However, the main drawback of AC microgrids is that they require a further AC/DC stage in every charging station, which decreases the efficiency of the overall system. Moreover, control in AC microgrids is complex, because it needs to keep the power factor into regulation levels. On the other side, DC microgrids just need a first rectification stage from the MV upper grid, removing the need for further AC/DC conversion stages per each charging station, which increases the efficiency of the overall system. Furthermore, control in DC microgrids is easier than in AC microgrids, because it does not have to deal with reactive power. Despite these advantages, the main drawback of DC microgrids is that there is no protection coordination standard, even though DC protection devices already exist. Another disadvantage is that there is no standard about accuracy and calibration of DC meters. Hence, DC protections and meters are challenges

that companies and research institutes need to face in order to widespread the use of DC microgrids for DC fast charging station systems. The difference between AC connected fast charging systems and DC connected fast charging systems is shown in Fig.1.

DC fast charging stations are currently available on the market with a power range from 30 to 400 kW. The output voltage is instead between 50 and 950 V, whereas the output current varies between 31.5 and 500 A. Due to the lack of protection and metering standards, most of them have been designed to be connected to the AC grid. Tritium PKM150 is instead an example of DC fast charging station designed to be connected to a DC microgrid. Its augmented efficiency compared to most of the other DC fast charging stations proves that the DC microgrid concept will play a key role in the future of EVs charging.

Due to their high power transfer, DC fast charging stations might require an upgrade of the existing grid infrastructure. This might happen especially in the countryside and highways, where DC fast charging stations are demanded for long-distance trips. In order to reduce grid reinforcement costs, it is possible to use energy storage systems (ESSs). ESSs can also help to reduce operational costs due to demand charges because they can be charged at low power compared to the power of DC fast charging stations. Moreover, ESS can be used to connect RESs with EV fast charging stations, which is a step forward toward the green energy transition.

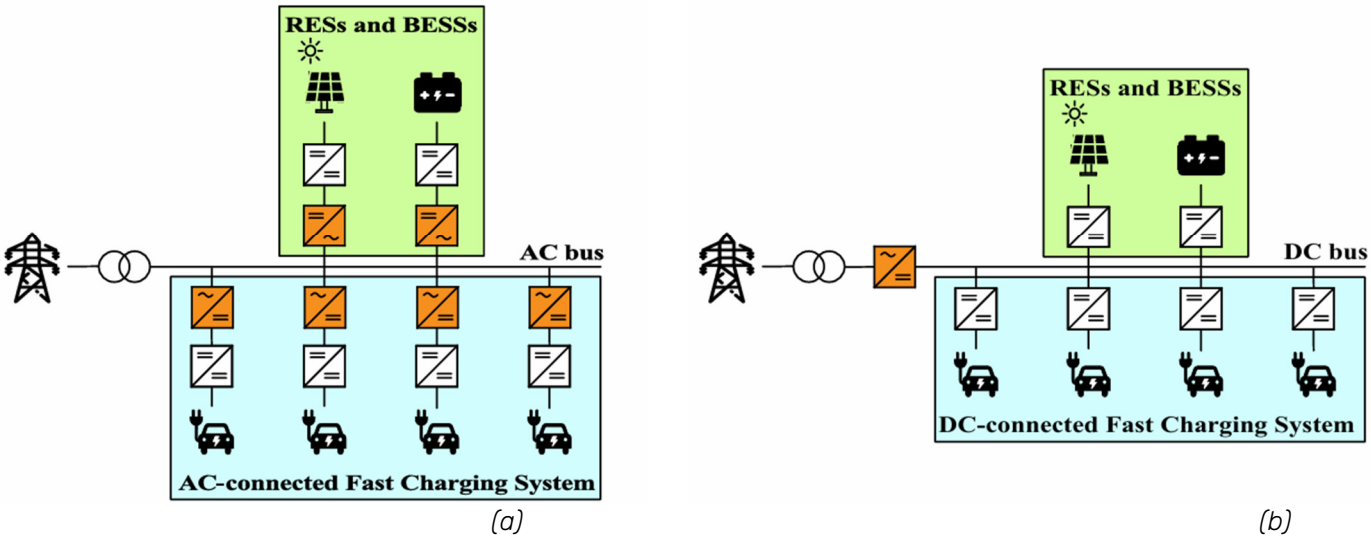


Fig. 1- DC fast charging infrastructure. (a) AC-connected fast charging system. (b) DC-connected fast charging system.

An important point to consider when designing DC fast charging stations is to provide isolation from the AC grid, in such a way as to avoid the propagation of a fault. The alternatives to reach this goal are to use a low-frequency transformer before the rectification stage or to use isolated DC-DC converters made of high-frequency transformers. The advantage of high-frequency transformers is that they are smaller and cheaper compared to low-frequency ones. Moreover, a low-frequency transformer can be seen as a single point of failure for the system and if it is damaged it is not possible to use any charging station connected to it. Furthermore, an architecture with a low-frequency transformer limits the operating switching frequency and makes the size and costs of the passive filters higher. On the other hand, high-frequency transformers influence soft-switching conditions and particular attention must be taken in their design.

DC Fast Charging of Electric Vehicles: Power Conversion Technology

Power electronics is the technology that enables the power transfer capability of EV charging stations. In particular, DC fast charging stations are made of two power conversion stages, respectively AC-DC and DC-DC. For this reason, this section aims to review the main AC-DC and DC-DC converters used in DC fast charging applications.

AC-DC converters

The three-phase PWM rectifier is a boost-type bidirectional topology made of three half-bridges, each of them with two switching devices, typically IGBTs or MOSFETs. This topology enables unity power factor and low total harmonic distortion (THD) thanks to its high controllability and capability to decouple active and reactive power. This topology is commonly preferred over the traditional diode rectifier, which is not considered a suitable choice for DC fast charging stations because of its high input harmonic content. So, the diode rectifier absorbs reactive power from the grid, which cannot be mitigated due to the lack of controllable switches. This phenomenon reduces the efficiency and deteriorates the grid voltage, which would represent a big issue because of the increasing spread of EVs and EV charging stations. The three-phase PWM rectifier is shown in Fig. 2.a

The neutral-point-clamped (NPC) rectifier is another boost-type AC-DC converter suitable for DC fast charging stations. In comparison to the three-phase PWM rectifier, it has two additional switches and two diodes per each leg, used to clamp the output voltage to the neutral point voltage. This topology has some advantages compared to the three-phase PWM rectifier. To start with, the voltage on the switching devices is only half of the DC-bus voltage. This means that there is less stress on the switching devices and that this topology has a double power rating than a three-phase PWM rectifier. Moreover, the THD of the NPC topology is lower than the one of the three-phase PWM rectifier. This topology allows the creation of a bipolar DC-bus. However, the presence of a bipolar DC-bus implies the need to balance the voltage of the neutral point through a proper control technique and/or additional balancing circuitry in case of load differences. So, the need for voltage balancing and the increased number of switches make the NPC rectifier control more complex than the three-phase PWM rectifier one. The NPC rectifier is shown in Fig. 2b.

The Vienna rectifier is a unidirectional topology made of a diode rectifier and three bidirectional switches. This topology provides very low THD, high power density, and high efficiency. Moreover, the switching devices are affected only by half the blocking voltage stress, because of the neutral point as in the NPC converter. The bidirectional version of this topology is the t-type converter, which substitutes the diode bridge with a three-phase PWM rectifier. The t-type converter keeps the advantages of the Vienna rectifier and allows the vehicle-to-x (V2X) operation mode, making it a suitable candidate for DC fast chargers of EVs. The Vienna rectifier and t-type converter are shown respectively in Fig 2c and Fig. 2d.

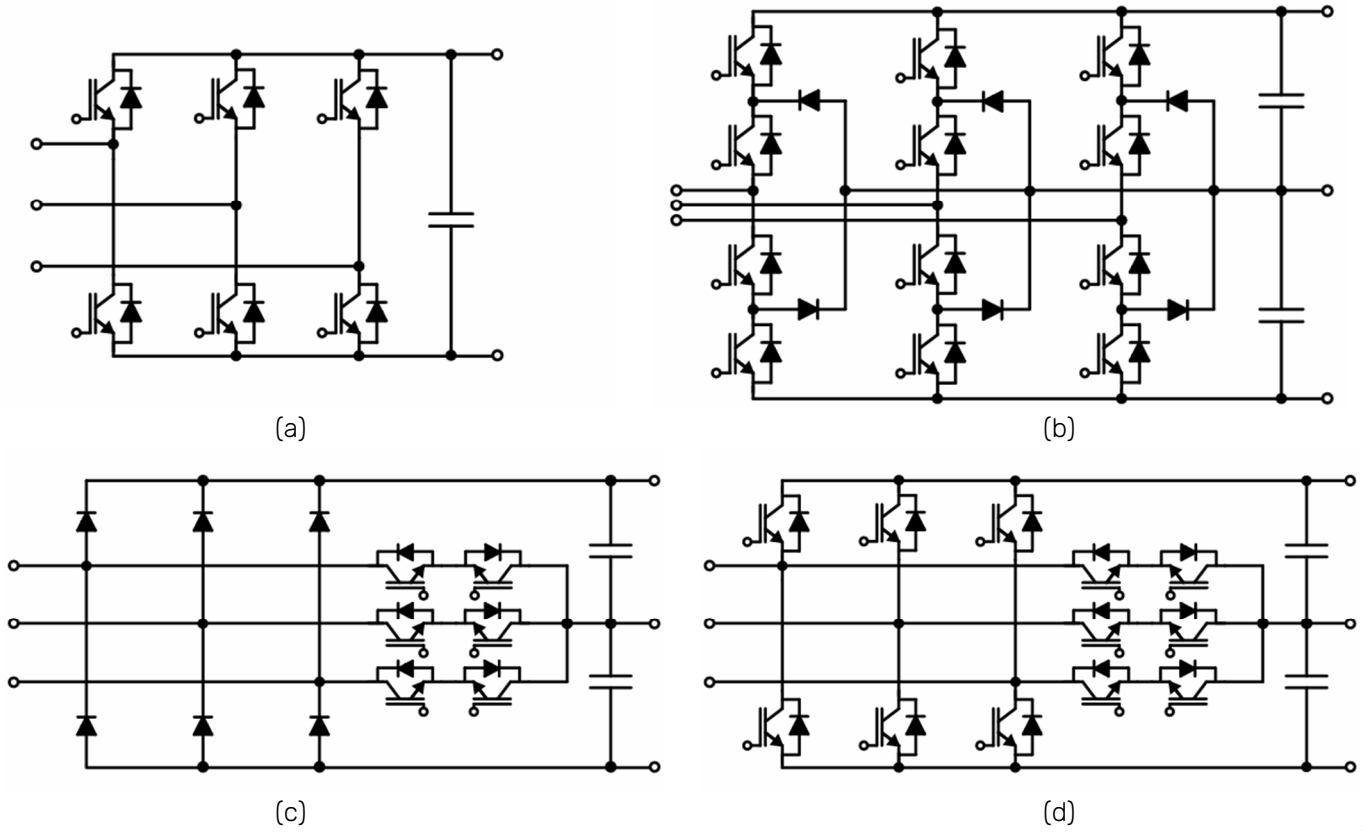


Fig. 2 - AC-DC power converters. (a) Three-phase PWM rectifier. (b) Neutral-point-clamped rectifier. (c) Vienna rectifier. (d) T-type converter

SMARTGYSUM project has been funded by the European Commission's Horizon 2020 Programme

DC-DC converters

The phase-shift full-bridge (PSFB) is a unidirectional topology suitable for high-power and high-voltage applications such as DC fast charging stations. This converter is an isolated topology, and it is made of a high-frequency transformer, a full bridge on the first side, and a diode bridge on the second side. The leakage inductance of the transformer enables the zero-voltage switching (ZVS) condition on the turn-on state of the switching devices. However, ZVS cannot be reached for low load currents because the ZVS condition of this topology is that the energy stored in the leakage inductance must be greater than the one stored in the output capacitance. The PSFB is shown in Fig. 1a.

The dual active bridge (DAB) is a well-known bidirectional topology, used in many applications, such as microgrids, aerospace, battery interface, and automotive, especially as on/off-board battery charger for EVs. In addition to its bidirectional power flow, this topology is appealing because of its galvanic isolation, high power density, high voltage gain, and capability to perform soft switching through proper modulation techniques. The DAB is made of two full bridges, connected through an isolation transformer. The series inductance of the transformer is designed to establish the power transfer of the converter itself. The DAB is shown in Fig. 1b.

Series resonant converters (SRCs) are a family of converters identified by a high-frequency transformer to guarantee galvanic isolation, and a series resonant tank made of an inductor and a capacitor. The first side can be a half-bridge, full-bridge, or even a multilevel half/full-bridge. The second side is a diode bridge in case of unidirectional topologies or typically equal to the first side in case of bidirectional topologies. The switching frequency of these converters can be chosen as the same, higher, or lower than the resonant frequency. However, it is recommended to choose the switching frequency equal to, or slightly above the resonant frequency to reach the soft-switching conditions. In addition to their soft-switching capability, SRCs are also chosen for their fault-tolerance feature. These features make these converters appealing for DC fast charging applications. A unidirectional SRC and a bidirectional one are shown respectively in Fig. 1c and Fig. 1d.

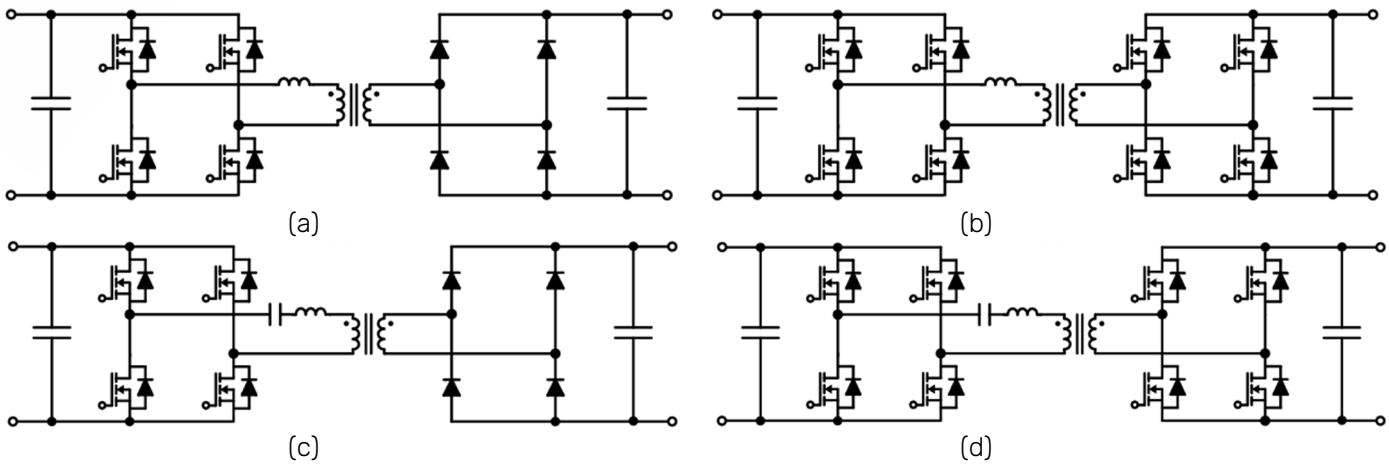


Fig. 1 - DC-DC power converters. (a) Phase-shift full-bridge. (b) Dual active bridge. (c) Unidirectional series resonant (d) Bidirectional series resonant converter

Four-Switch Buck-Boost and Dual Active Bridge Converters

The working principle of the four-switch buck-boost and dual active bridge converters will be explained in this paragraph to have a comparison between an isolated and a non-isolated topology. The comparison was originally made for an AC charging application but the converter topologies can be rated for higher power to match DC fast charging applications.

Four-Switch Buck-Boost

The idealized circuit diagram of a Four-Switch bidirectional Buck-Boost converter is shown in Fig. 2a. It is a non-isolated converter which benefits from a low number of switching elements and a simple design and control. With D_1

as the duty cycle of S_1 (while $S_2 = \bar{S}_1$) and D_2 as the duty cycle of S (while $S_3 = \bar{S}_4$) the voltage gain of the FSBB can be expressed with:

$$\frac{V_{DC2}}{V_{DC1}} = \frac{D_1}{1 - D_2} \quad (1)$$

The FSBB can be used in buck, boost, or buck-boost mode. From the ratio (1) it can be derived that if D tends to zero the FSBB gets Buck property, whereas it gets Boost property for D tending to zero. In this paper, the FSBB is used in Buck and boost modes by respectively setting D_2 =0 and D_1=1. It allows also a current flow directly from one side to the other by simultaneously setting D_1=1 and D_2 =0.

Dual Active Bridge

DAB is one of the most widespread converters in DC microgrids and automotive applications. Even though it was firstly proposed in the early 1990s, losses due to old technologies of power devices resulted in low efficiency. However, it gained popularity after the development of silicon carbide (SiC) and gallium-nitride (GaN) switching devices, making it appealing for power grid applications. The features that make this converter so appealing are the galvanic isolation, wide voltage gain range, and capability to perform soft-switching through proper modulation techniques.

As shown in Fig. 2, the Dual Active Bridge is composed of two full bridges, connected to two voltage sources. This is a typical case of a ESSs connected to a DC grid through a medium or high frequency transformer to guarantee the galvanic isolation. The inductor L is modeled in series to the transformer and represents the sum of the leakage inductance of the transformer and an external inductor, which is designed to achieve a certain power transfer. The phase shift angle between the gate control signals of the two full bridges is used to regulate the power transfer of this converter, which can be described by:

$$P_{DAB} = \frac{n\, V_{DC1} V_{DC2}\, \varphi(\pi - |\varphi|)}{2\, f_s\, \pi^2\, L}, \quad \forall -\pi \leq \varphi \leq \pi \quad (2)$$

where n is the turn ratio N_1/N_2 and f is the switching frequency. The total inductance of the converter can be designed from (2) by imposing a maximum power transfer and a maximum phase shift angle.

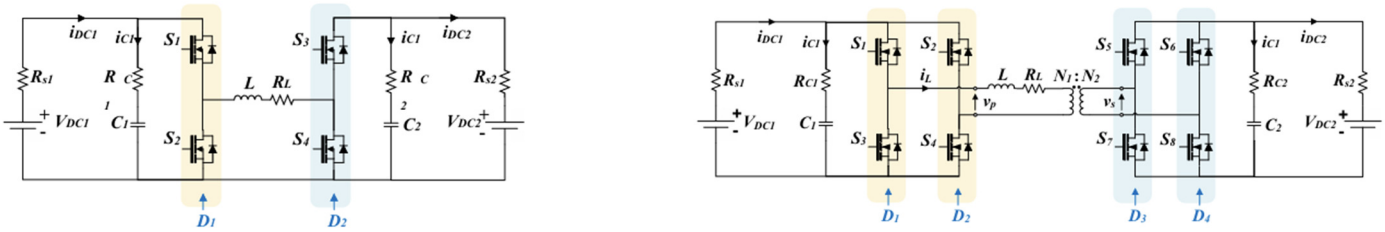


Fig. 2 - Converter Topology: (a) four-switch buck-boost, (b) dual active bridge

Converter Losses

In this section, the loss analysis for both converters is reported. During the switching process of a SiC-MOSFET, energy losses occur due to the simultaneous presence of drain-source voltage and drain current. These losses are called switching losses. Due to the approximately triangular rise and fall of the drain-source voltage, the switch energy losses can be approximated by:

$$P_s = \frac{1}{2}\, V_{DS}\, I_D\, (t_r + t_f)\, f_s \quad (3)$$

where V_{DS} is the drain-source voltage and I_D is the RMS value of the drain current. Conduction losses in switching components can be modeled with an equivalent series resistance R_{on}. Hence, the conduction losses can be calculated with:

$$P_{cond,on} = R_{on} I_D^2 \quad (4)$$

where R_{on} is the equivalent series resistance of semiconductor. To prevent a short circuit of two series SiC-MOSFETs, a dead time t_{dead} is used between the turn-on and the turn-off of the two switches respectively of the same leg.

During this time the current forced by the inductance flows through the body diode of the low-side SiC-MOSFET. The dead time losses P_{dead} is calculated as:

$$P_{dead} = V_{diode}\, I_{diode}\, t_{dead}\, f_s \tag{5}$$

where V_{diode} is the forward voltage of the diode and I_D is the RMS value of the diode current. The inductor contributes essentially with conduction losses, converting electrical energy into heat due to the inductor resistive behavior. To represent these losses, a series DC resistance R_L has been modeled and hence calculated with:

$$P_L = R_L I_L^2 \tag{6}$$

where I_L is the RMS value of the inductor current. The capacitor losses, caused by leakage and dielectric loss, can also be modeled with an equivalent series resistance R_C and calculated in the same way as for inductor conduction loss in (6). Finally, the transformer losses for the DAB can also be modeled with a series resistance R_T , neglecting the magnetic losses. The total power loss The total power loss was modelled as a superposition. The efficiency is thus expressed by equation (7).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + \sum\left(P_S + P_{cond,on} + P_{dead}\right) + P_R} \tag{7}$$

where P_R is the sum of the resistor losses related to inductors, capacitors and transformer.

Short-circuit analysis

Subsequently , the short-circuit behaviour of the FSBB converter was analysed for both low-voltage (LV) and high-voltage (HV) side faults, distinguishing between buck and boost operating modes. In boost mode, the fault current results from three concurrent contributions: the discharge of the filter capacitors, the freewheeling current forced through the diodes by the inductor, and the feeding from the input source through the diodes. Without any additional protection mechanism, the fault current in boost mode would grow unbounded. However, the FSBB exhibits a useful intrinsic property: when a short circuit occurs on the HV side, the collapse of the HV voltage causes the converter to switch automatically into buck mode, which suppresses the fault current contribution from the input source. The LV-side current during an HV fault is therefore inherently limited, a behaviour that distinguishes the FSBB from a conventional boost converter. Simulation results confirmed this mechanism, showing an exponential capacitor discharge on the faulted side and effective current suppression on the non-faulted side, with the mode-switching control playing a critical role.

For the DAB converter, the short-circuit analysis was carried out in open loop to demonstrate the converter's natural fault-riding capability. Results for both LV and HV faults showed that the dominant fault current contribution again comes from the filter capacitors, but the DAB is able to bring its fault current contribution to zero within milliseconds, without any dedicated control action. This behaviour stems from the galvanic isolation provided by the high-frequency transformer, which intrinsically decouples the two sides of the converter. The analysis confirmed that the DAB is inherently safer than the FSBB under fault conditions, since it does not rely on a mode-switching mechanism to limit the fault current — a mechanism that, in the FSBB, could fail in the event of a control or measurement malfunction.

Overall, the comparison showed that both converters are capable of suppressing fault currents in the millisecond range, but through fundamentally different mechanisms: the FSBB through a control-dependent mode switch, and the DAB through its structural isolation.

Numerical integration methods for DAB simulation

Afterwards the numerical integration methods for fixed-step simulation of the DAB converter have been investigated, with particular relevance to real-time digital simulators such as OPAL-RT, where only fixed-step explicit methods are applicable. Four methods were considered, spanning first to fourth order: Euler, Heun, Bogacki-Shampine, and Runge-Kutta. Two DAB configurations were simulated, differing in switching frequency (10 kHz and 1 kHz) and inductance value, with the ode45 variable-step solver used as reference.

The results showed that the Bogacki-Shampine method (third order) provided the best accuracy across both configurations and time steps, with its output voltage curve nearly superimposed on the ode45 reference in most cases. The Runge-Kutta method (fourth order) did not consistently surpassed in performance Bogacki-Shampine, which means that a higher integration order does not automatically guarantee better accuracy. A further notable finding was that the optimal choice of method depends on the specific converter parameters: for the 1 kHz configuration, even the first-order Euler method produced results close to the ode45 reference, whereas for the 10 kHz configuration the same method showed larger deviations.

Regarding computational cost, the Euler method was by far the fastest, making it the most suitable candidate for real-time applications where simulation time is a hard constraint and moderate accuracy is acceptable. Higher-order methods required significantly longer computation times — Runge-Kutta was approximately three to four times slower than Euler at the same time step — while ode45, being a variable-step solver, was competitive at small time steps but slower at larger ones.

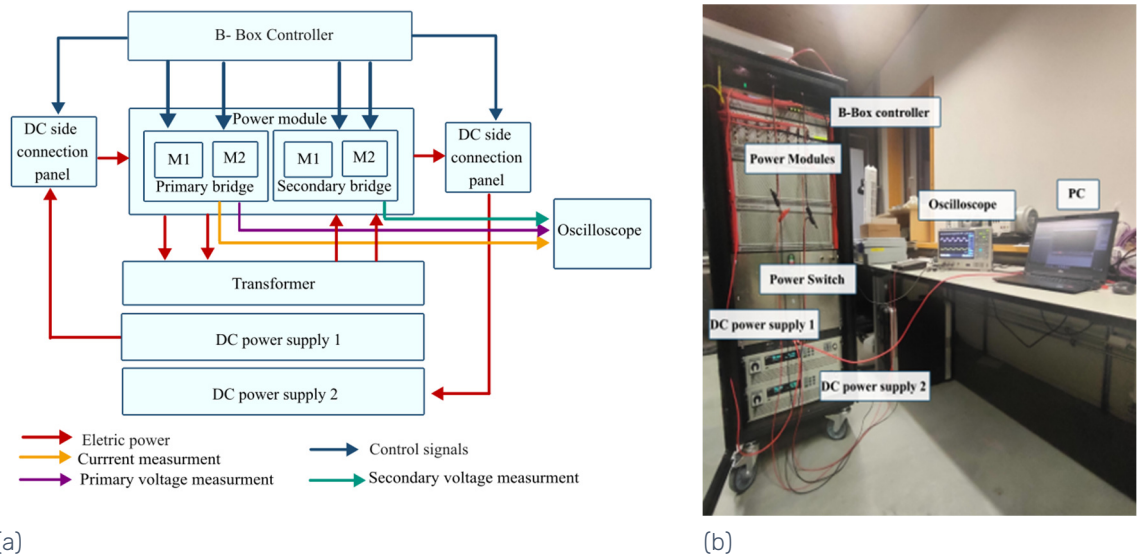
Experimental Validation of the DAB Converter for Wide Voltage Range Operation

The theoretical investigations described in the previous sections culminated in an experimental campaign conducted from November 2023 to February 2024 at the Energy Lab 2.0 of the Karlsruhe Institute of Technology. The objective was to test the behaviour and efficiency of an 8 kW DAB converter over a wide output voltage range of 400–800 V, using a bidirectional DC power supply as an active load to simulate EV battery behaviour.

The introduction of 800 V EV platforms on the market has created a demand for DC-DC converters capable of operating across a wide output voltage range. A 400 V charger cannot directly serve an 800 V EV without an additional 1:2 step-up converter on the vehicle side, which introduces extra conversion losses. The DAB converter is one of the most widely adopted solutions in DC fast charging stations due to its bidirectional power flow, galvanic isolation, high power density, and soft-switching capability. However, it is known to lose the zero-voltage switching (ZVS) condition when operating far from the nominal transformer turns ratio. This experiment was designed to quantify this limitation.

Prototype hardware

The experimental setup was realised using commercial hardware from Imperix. The power stage consisted of PEB8024 half-bridge power modules, each featuring 1200 V SiC MOSFETs (Cree C2M0080120D) with a maximum drain-source current of 31.6 A and a switching frequency range of 1–200 kHz. Four modules were used to build the two full bridges of the DAB. A 1:1 high-frequency transformer was connected in series with a total inductance of 64 µH, obtained by connecting four 16 µH inductors to each terminal of the transformer. The controller was an Imperix B-Box, based on a Xilinx Zynq XC7Z030 SoC combining an ARM Cortex-A9 dual-core processor at 1 GHz with a Kintex-7 FPGA, and providing optical PWM outputs at up to 50 Mbps.



(a) (b)

Fig. 3 - Experimental setup. (a) Schematic diagram of the prototype. (b) Real experimental setup.

The primary-side DC power supply provided the input power, while the secondary-side supply acted as active load. Between each supply and the power modules, a DC-side connection panel was inserted, comprising a 30 A fuse, a precharge resistor, a precharge relay, and a bypass relay, to limit inrush currents at startup.

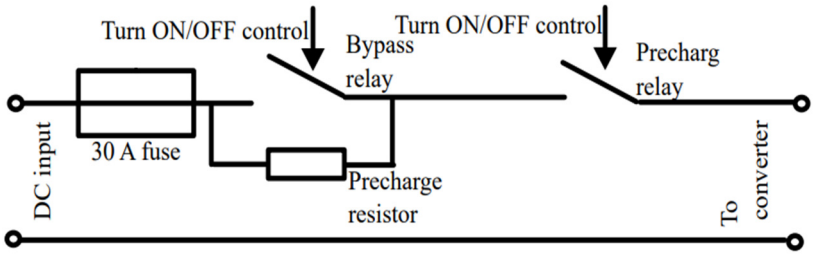


Fig. 4 - DC side connection panel.

Soft-start procedure

A two-stage soft-start sequence was implemented to avoid inrush currents that could trigger half-bridge protections or cause permanent damage. Upon receiving a start signal, the DC-side connection panel first closes the precharge relays; after 1.1 s, the bypass relays are also closed. The primary bridge is activated only after both relay stages are complete: its internal phase shift between the two legs starts at 0° and ramps up to 180° over 0.9 s, progressively increasing the power transfer. The secondary bridge is then fully activated 1 s after the primary bridge reaches steady state. When a stop signal is received, the converter returns to standby.

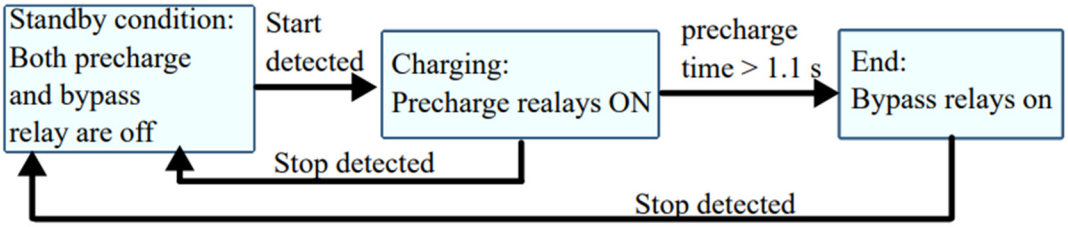


Fig. 5 - Soft starting procedure of the DC side connection panel

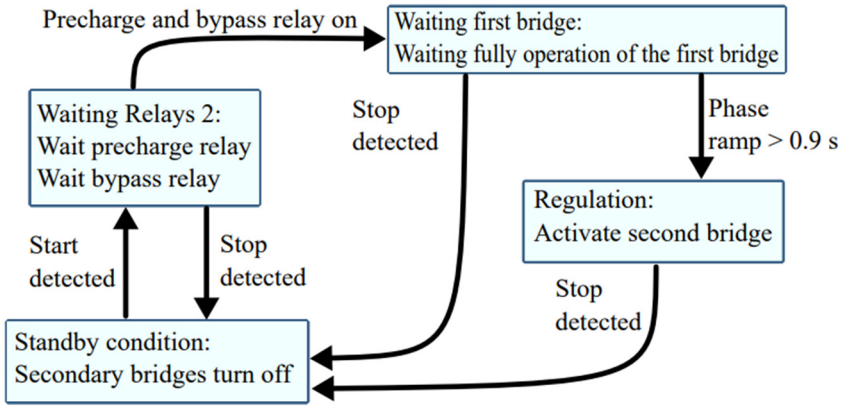


Fig. 6 - Primary bridge soft starting procedure

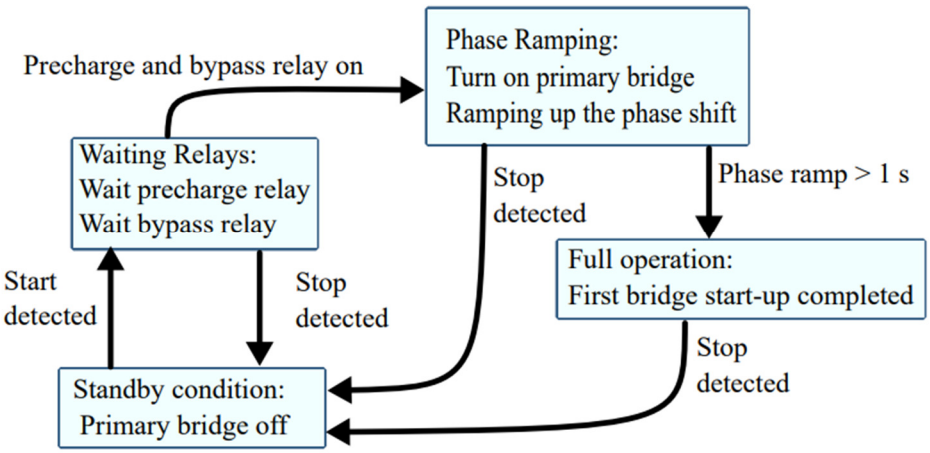
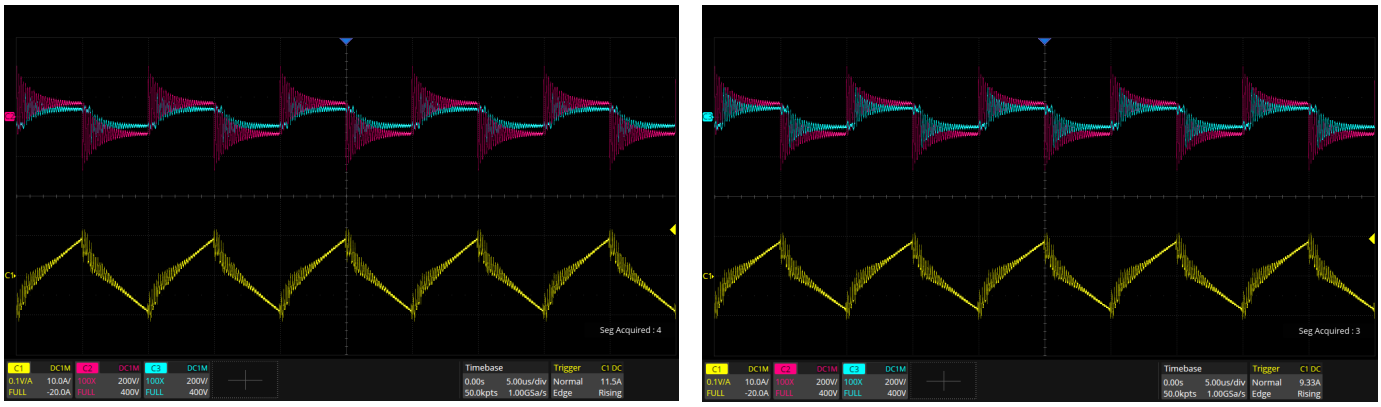


Fig. 7 - Secondary bridge soft starting procedure

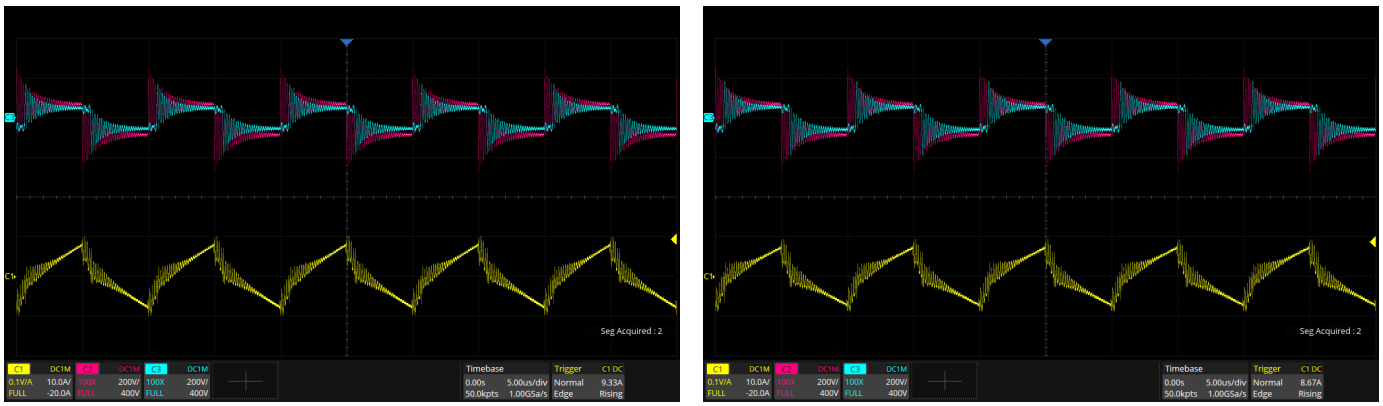
Experimental results

The experiments were carried out in open loop at a fixed input voltage of 800 V, sweeping the output voltage from 400 V to 800 V in 50 V steps. At each operating point, the primary and secondary transformer voltages and the inductor current were recorded via oscilloscope probes.



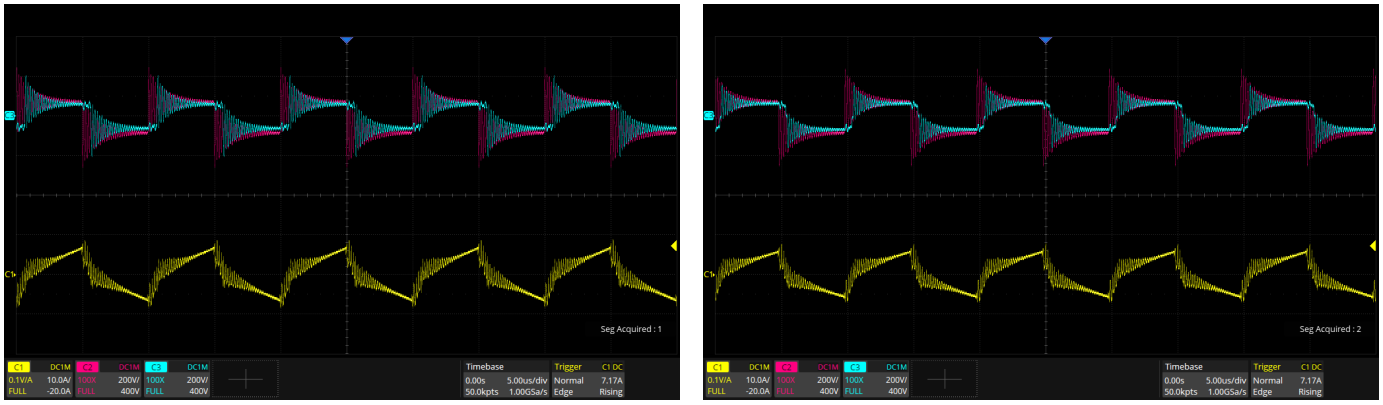
(a) *(b)*

Fig. 8 - DAB waveforms. (a) 800 V Input, 400 V Output. (b) 800 V Input, 450 V Output



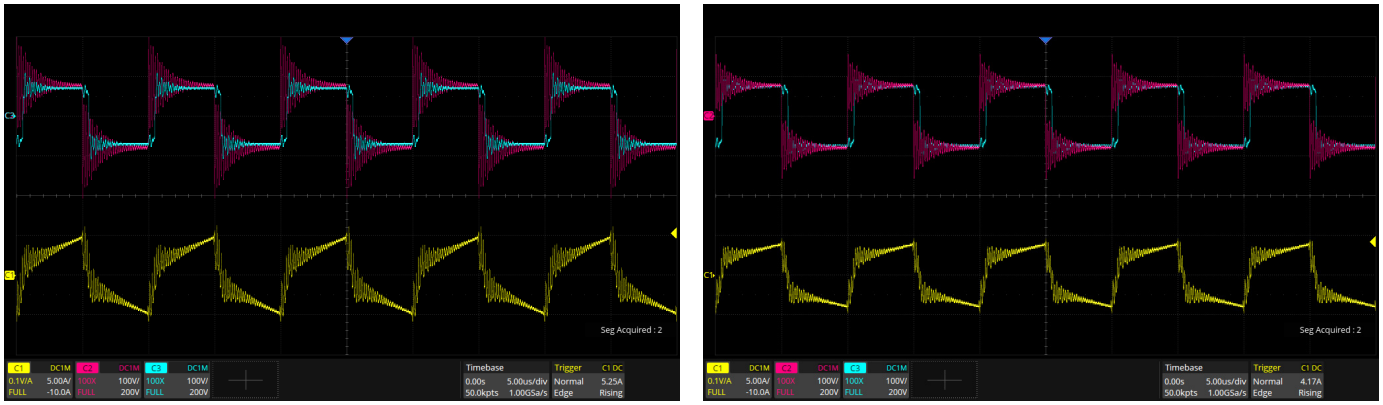
(a) *(b)*

Fig. 9 - DAB waveforms. (a) 800 V Input, 500 V Output. (b) 800 V Input, 550 V Output



(a) (b)

Fig. 10 - DAB waveforms. (a) 800 V Input, 600 V Output. (b) 800 V Input, 650 V Output



(a) (b)

Fig. 11 - DAB waveforms. (a) 800 V Input, 700 V Output. (b) 800 V Input, 750 V Output

Fig. 12 - DAB waveforms. 800 V Input, 800 V Output

The waveforms clearly show increasing distortion as the output voltage moves away from the input voltage, confirming that the DAB loses ZVS at large voltage conversion ratios. At the nominal operating point (800 V / 800 V), the waveforms are clean and soft-switching is maintained. At the most asymmetric point (800 V / 400 V), the waveforms are significantly distorted.

The measured input and output power values across the voltage range are reported in the table below, together with the corresponding efficiency:

Table 1 - Experimental values of the DAB converter

Input voltage	Output voltage	Input Power	Output Power
800 V	400 V	2.66 kW	2.444 kW
800 V	450 V	2.942 kW	2.743 kW
800 V	500 V	3.228 kW	3.033 kW
800 V	550 V	3.512 kW	3.319 kW
800 V	600 V	3.786 kW	3.597 kW
800 V	650 V	3.799 kW	3.660 kW
800 V	700 V	3.709 kW	3.602 kW
800 V	750 V	3.7 kW	3.615 kW
800 V	800 V	3.732 kW	3.65 kW

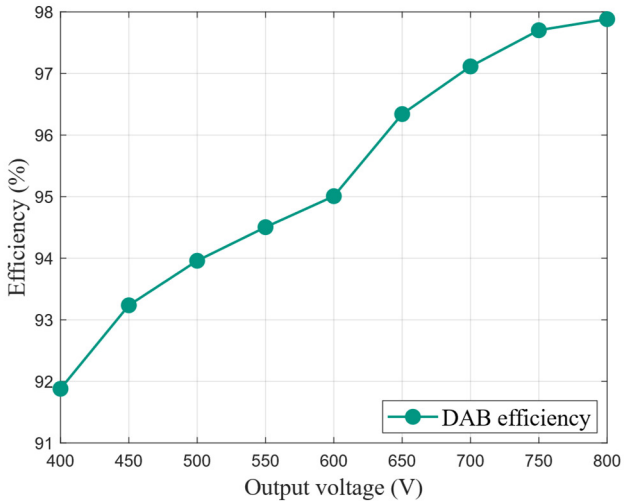


Fig. 13 – DAB efficiency over a wide voltage range.

The efficiency drops from approximately 97.8% at the nominal 1:1 voltage ratio to 91.9% at the 2:1 ratio (800 V / 400 V). This confirms that the DAB converter, when operated with single-phase-shift modulation, is not suitable as a standalone solution for wide-range EV charging applications. Maintaining high efficiency across a 2:1 voltage range requires either advanced modulation strategies (e.g. extended or dual phase shift), or the use of multiple DAB modules in series/parallel configurations. These results directly motivated the investigation of more flexible architectures reviewed in the DC fast charging survey [Arena et al., 2024], and establish quantitative benchmarks for the comparison of alternative converter topologies.

3.4.3. Scientific outcomes (ESR08 - Danilo Di Berardino)

Context and Motivation

The he most widely adopted renewables sources, such as PV and wind turbines, are inherently characterized by intermittent power production, often associated with high seasonal variability. Battery systems, while suitable for short-term storage, are impractical for storing large amounts of energy, due to self-discharge, degradation, and the prohibitive cost related to the capacity required. Especially in remote communities, islands, and off-grid industrial sites, diesel generators are the typical solution, resulting in high operational costs and significant CO_2 emissions.
Hydrogen-based energy storage (HES) offers a compelling alternative for long-duration storage: hydrogen can be produced via electrolysis during periods of excess renewable generation, compressed, stored at high pressure, and subsequently converted back to electricity through a fuel cell when demand exceeds local generation. The overall round-trip efficiency is lower than that of batteries, but the volumetric energy density and the negligible self-discharge of hydrogen storage make it uniquely suited for seasonal applications

Despite the theoretical suitability of HES for off-grid seasonal storage, the conditions under which hydrogen storage becomes economically competitive with respect to diesel generators or battery-only alternatives are not yet well-characterised for small-scale residential applications. This gap motivates the feasibility assessment carried out in this first stage of the work.

Research Objectives

The primary objective of this research phase is to determine, through a systematic techno-economic analysis, under which conditions a hybrid energy system, which include PV, battery, and hydrogen storage system is economically competitive with a diesel-generator-based alternative for supplying an off-grid residential neighbourhood. The specific objectives are: (i) to develop a MATLAB-based tool for the automated sizing and economic assessment of hybrid HES; (ii) to apply the tool to a realistic off-grid residential scenario using measured load and irradiance data; (iii) to compare the resulting levelized cost of electricity (LCOE) against the equivalent diesel generation cost across multiple European geographic locations and under component cost sensitivity scenarios; and (iv) to identify the

conditions (irradiance levels, component costs) and the critical parameters (most relevant devices cost) under which hydrogen storage becomes economically viable.

System Description

The studied system is a hybrid energy storage system composed of the following components: a PV plant (the sole energy source), a battery bank, an alkaline electrolyser (AEL), a hydrogen compressor, a pressurised hydrogen storage tank (15 MPa), and a PEM fuel cell. The system is designed to supply an off-grid residential neighbourhood of 10 single-family households in a fully self-sufficient manner, with no connection to the main electrical grid. The base case dataset is drawn from the WPuQ project, which provides high-resolution electric load profiles (up to 10-second resolution) measured from an enclosed residential district near Hamelin, Lower Saxony, Germany. The dataset covers September 2020 to August 2021 (8784 hours), corresponding to a full year of operation. Load data from 10 households were selected as the representative base case.

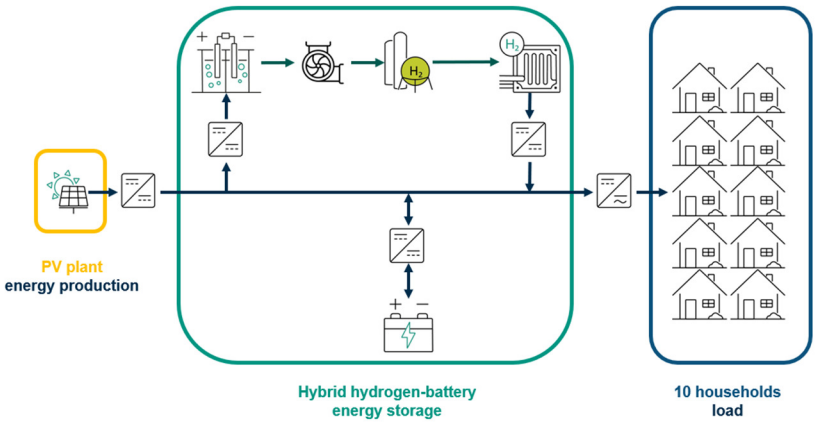


Fig. 14 – Diagram of the system under study

As a reference alternative, a diesel-generator-based system is considered. The diesel generator is sized according to the maximum load demand plus a 20% safety margin. Two diesel price scenarios are considered: 1.5 €/L (Heizöl, tax-exempt heating oil) and 2.0 €/L (standard transportation diesel). Operational expenditure (OPEX) costs for the diesel system increase at 2% per year, reflecting fuel price escalation and generator maintenance.

Sizing Methodology and MATLAB Tool

A MATLAB tool was developed to perform the sizing and simulation of the hybrid HES. The sizing procedure is structured in two stages. The first stage consists of a manual optimization: a PV sizing function determines the required PV peak power as a function of two user-defined parameters: (a) the production factor, defined as the ratio between annual energy produced by the PV plant and annual energy demanded by the load; and (b) the required storage efficiency, defined as the weighted average efficiency of the battery and the hydrogen storage subsystem. These two parameters directly control the relative sizes of the battery and the hydrogen storage system. Based on the production factor, the PV size is determined iteratively; the battery is then sized to match the required storage efficiency; and the electrolyser, compressor, hydrogen tank, and fuel cell are sized accordingly, proportional to the nominal load power and PV capacity.

In the second stage, a Particle Swarm Optimization (PSO) algorithm is applied to minimise the total system LCOE over the 20-year economic horizon. The PSO searches over the space of production factor and required storage efficiency to find the combination that yields the minimum cost while guaranteeing full off-grid energy autonomy. A derating correction factor is included in the optimisation to account for the reduction in PV output due to temperature, soiling, and ageing. In a further refinement step, component sizes are discretized to commercially available standard sizes, reflecting the real-world constraint that devices are not available at arbitrary capacities.

The energy flow management during simulation follows a simple rule-based strategy based on battery priority: the battery is always charged or discharged first, to the maximum possible extent, before the hydrogen storage system is engaged. This strategy minimises hydrogen cycling and maximises the use of the more efficient battery storage.

Economic Assessment Framework

The economic assessment spans a 20-year project lifetime. Capital expenditure (CAPEX) is computed from the device sizes and cost-per-unit values derived from literature and from actual devices available at the KIT Energy Lab (used as reference for the electrolyser, compressor, and fuel cell). Operational expenditure (OPEX) includes annual maintenance costs, modelled as a fixed percentage of CAPEX for each device. The key economic metrics computed are: the Net Present Value (NPV), the Levelised Cost of Electricity (LCOE), and an equivalent diesel price, defined as the diesel fuel price at which the 20-year cost of the diesel-generator alternative equals the NPV of the HES. This last metric provides a concise and intuitive indicator of economic competitiveness: if the actual diesel price exceeds the equivalent diesel price, the HES is more economical than the diesel alternative.

Table 2 - Devices reference cost and reference cost per unit

Device	Size	Cost	Cost per unit	Source
Photovoltaic plant	100 kW	62 800 €	628 €/kW	Scientific literature
Battery	300 kWh	63 000 €	210 €/kWh	Scientific literature
Electrolyzer (AEL)	48 kW	86 982 €	1 812 €/kW	Energy Lab device
Compressor	16 kg/h	170 000 €	10 625 €/(kg/h)	Energy Lab device
Hydrogen tank (15 MPa)	20 m³	60 000 €	3 000 €/m³	Scientific literature
Fuel cell	10 kW	30 000 €	3 000 €/kW	Scientific literature

Minimum cost-per-unit values, representative of near-future projected costs, are used as the baseline scenario. These values are: PV at 400 €/kW, battery at 150 €/kWh, alkaline electrolyser at 400 €/kW, compressor at 7000 €/(kg/h), hydrogen tank at 1855 €/m³, and PEM fuel cell at 900 €/kW. To assess cost sensitivity, two additional scenarios are tested: a pessimistic case with all costs increased by 50%, and an optimistic case with all costs reduced by 50%.

Results and Discussion

Table 3 – Summary of the results

Scenario	Location	LCOE (€/kWh)	Total CAPEX (k€)	OPEX yr1 (k€)	Equiv. diesel price (€/L)	Notes
Battery-only (manual)	Germany	5.236	3 499	69.4	N/A	No H2; 22.8 MWh battery; LCOE ~15x higher than hybrid
Hybrid HES (manual sizing)	Germany	1.008	652	15.0	N/A	Manual sizing, no PSO optimisation
Hybrid HES (PSO, diesel 2 €/L)	Germany 2019-20	0.631	438	8.5	N/A	PSO optimised; HES cheaper than diesel at 2 €/L

Hybrid HES (PSO, diesel 1.5 €/L)	Germany 2019-20	0.682	438	8.5	N/A	PSO optimised; HES still more expensive at 1.5 €/L
Hybrid HES (PSO + derating)	Germany 2019-20	0.674	465	9.2	2.04	PV derating correction included
Hybrid HES (PSO + derating + discretized)	Germany 2019-20	0.695	480	9.3	2.04	Commercially available device sizes
+50% cost sensitivity	Germany 2019-20	0.992	687	13.2	2.93	All component costs x1.5; HES competitive only at high diesel price
-50% cost sensitivity	Germany 2019-20	0.577	397	7.9	1.69	All component costs x0.5; competitive with Heizoil pricing
Hybrid HES (PSO + derating)	Sweden 2019-20	0.959	657	13.3	2.84	Lower irradiance; larger H2 tank required
Hybrid HES (PSO + derating)	Sweden TMY	0.960	663	13.0	2.82	Typical meteorological year
Hybrid HES (PSO + derating)	Ginostra TMY	0.438	305	5.7	1.27	High irradiance island; competitive with island diesel prices
PV + battery only (PSO)	Caltanissetta 2019-20	0.331	238	3.8	N/A	PSO converges to zero H2; LCOE below grid price (0.352 €/kWh)

Table 3 summarises the key results for all scenarios investigated. The base Germany scenario (2019–20 irradiance data, PSO-optimised with derating correction) yields an optimal system with 418 kW of PV, 481 kWh of battery capacity, 23 kW of electrolyser, 37.9 m³ of hydrogen storage, and 22.8 kW of fuel cell. The total CAPEX is approximately 465 k€, with OPEX of 9.2 k€/year in the first year. The resulting LCOE is 0.674 €/kWh and the equivalent diesel price is 2.04 €/L. This means that the HES is more economical than a diesel generator when diesel costs more than approximately 2.04 €/L, which is consistent with standard transportation diesel prices in Germany. After discretization to commercially available device sizes, the LCOE increases slightly to 0.695 €/kWh.

For comparison, a battery-only storage system for the same off-grid scenario in Germany requires approximately 22.8 MWh of battery capacity, leading to a LCOE of 5.24 €/kWh. The dominant cost in the HES is the hydrogen storage tank, which accounts for approximately 19–24% of total CAPEX depending on the scenario, followed by the PV plant and the battery.

The geographic sensitivity analysis reveals a strong dependence on local solar irradiance. For Sweden (lower irradiance), the LCOE rises to approximately 0.96 €/kWh and the equivalent diesel price to 2.82–2.84 €/L. In contrast, for Ginostra (a small island in southern Italy, high irradiance), the LCOE drops to 0.438 €/kWh and the equivalent diesel price to 1.27 €/L — indicating that at typical Italian island fuel prices, the HES is already economically competitive. The most favourable result is obtained for Caltanissetta (Sicily, high irradiance, grid-connected reference): the PSO optimiser converges to a solution where the hydrogen subsystem is effectively sized to zero, resulting in a PV + battery-only system with LCOE of 0.331 €/kWh. This result indicates that hydrogen storage is not necessary in high-irradiance locations, PV + battery alone represents a more convenient solution.

Cost sensitivity analysis confirms that the cost of hydrogen storage components is the main driver of feasibility. A 50% reduction in all component costs (optimistic scenario, Germany) lowers the equivalent diesel price to 1.69 €/L, bringing the HES into competitive range with heating oil pricing in Germany. Conversely, a 50% cost increase raises the equivalent diesel price to 2.93 €/L, showing that, despite not economically viable, the equivalent price remains within a comparable range. These results highlight that the hydrogen tank and electrolyser cost trajectories are the critical factors for future economic viability.

Outlook

The feasibility assessment presented here establishes the economic boundary conditions for hydrogen storage integration in off-grid microgrids and identifies the scenarios where it is most promising. Building on these results, the next phase of the research will focus on dynamic modelling of the selected reference scenario in

MATLAB/Simulink. A Simulink model of the hybrid HES will be developed, capturing the dynamic behaviour of the electrolyser, fuel cell, and power electronics interfaces. Different control strategies for energy management will be designed and compared, with particular attention to grid services provision (frequency regulation, peak shaving).

The validated Simulink model will subsequently serve as the basis for real-time implementation on a hardware-in-the-loop simulator. Experimental validation is planned using the H2-in-the-Loop (H2IL) facility at the KIT Energy Lab 2.0. Validation experiments will compare simulated and measured hydrogen system dynamics under representative load and generation profiles, and results will be fed back into the economic model to refine the OPEX estimates for services-providing scenarios.

3.4.4. Contribution to the WP objectives (ESR08 – Gabriele Arena)

The main results achieved during the first phase of IRP8 contribute to the WP3 objectives by advancing the understanding of power converter topologies and their suitability for DC network applications, with a particular focus on DC fast charging stations for electric vehicles as a representative and industrially relevant instance of distributed DC microgrids.

A comprehensive study of the DC fast charging landscape — covering standards, architectures, isolation schemes, and power conversion technology — established the technical requirements that DC-DC converters must fulfil in this application context. Against this backdrop, a comparative analysis between an isolated topology (the Dual Active Bridge) and a non-isolated one (the Four-Switch Buck-Boost) was carried out, examining efficiency, short-circuit behavior, and suitability for wide output voltage ranges. This comparison provided clear selection criteria for converter topologies in DC microgrid and fast-charging scenarios, directly supporting to identify efficient and robust power conversion solutions for smart energy distribution systems.

Building on this theoretical foundation, an experimental validation campaign was conducted on an 8 kW DAB converter setup. Open-loop experiments, supported by a soft-starting procedure to prevent inrush currents at startup, confirmed the converter's waveform behaviour and allowed its efficiency to be characterised across the operating range. A key finding emerged from this experimental work: the DAB converter, in its single-module configuration, exhibits a significant efficiency drop when operated over a wide output voltage range — such as that required by EV battery charging applications. This result has direct implications for system design, indicating that single-module DAB converters are not suitable for wide-range fast-charging duties and that series or parallel connection of identical modules is necessary to maintain high efficiency..
Moreover, the scientific work presented in this report contributes to the WP3 objectives through the evaluation of a DAB converter for DC fast charging applications, thereby addressing the integration of distributed energy storage systems — represented in this context by the energy buffers embedded in electric vehicles — into DC microgrid architectures.

3.4.5. Contribution to the WP objectives (ESR08 - Danilo Di Berardino)

The work carried out contributes to the WP3 objectives in two interconnected ways. The first stage of research surveys a broad range of off-grid configurations and hydrogen application contexts, narrowing them down to the most technically and economically representative scenario to be investigated through real-time analysis in the next phase. Building on this, the quasi-static simulation model and the PSO-based sizing results together constitute the reference case against which the real-time model will be benchmarked: the hourly energy balance and the optimised component sizing define the expected system behaviour, so that any deviation observed in the real-time simulator can be systematically interpreted as the effect of dynamic phenomena that are invisible at the quasi-static level. This comparison will thus quantify the added value of real-time modelling over simplified analysis.

3.4.6. Scientific achievements

Experimental prototypes

#	Name	Description	Status (designed, assembled, tested)	Photo
1	8 kW Dual Active Bridge setup	An 8 kW Dual Active Bridge setup from the Imperix Company. It has different inductor values in such a way to experiment different possible configurations.	Assembled	
2	20 kW Dual Active Bridge	A 20 kW Dual Active Bridge setup from the Imperix Company. It has different inductor values in such a way to experiment different possible configurations.	Assembled	

Publication

#	Title, incl. citation information	Type (Conference, journal, book chapter)	Status (Submitted, accepted, published)	DOI
1	Ö. Ekin, G. Arena, S. Waczowicz, V. Hagenmeyer and G. De Carne, "Comparison of Four-Switch Buck Boost and Dual Active Bridge Converter for DC Microgrid Applications," 2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Kiel, Germany, 2022, pp. 1-6	Conference	Published	10.1109/PEDG54999.2022.9923074
2	G. Arena, D. Vinnikov, A. Chub and G. De Carne, "Accuracy Analysis of Dual Active Bridge Simulations under Different Integration Methods," 2022 AEIT International Annual Conference (AEIT), Rome, Italy, 2022, pp. 1-6	Conference	Published	10.23919/AEIT56783.2022.9951711
3	G. Arena, P. Emiliani, A. Chub, D. Vinnikov and G. D. Carne, "DC Fast Charging of Electric Vehicles: a Review on Architecture and Power Conversion Technology," 2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE POWERENG), Tallinn, Estonia, 2023, pp. 1-6	Conference	Published	10.1109/CPE-POWERENG58103.2023.10227492
4	P. Emiliani, A. Blinov, G. D. Carne, G. Arena and D. Vinnikov, "Predictive Control for Isolated Matrix Rectifier Without Current Distortion at Sector Boundary," 2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE POWERENG), Tallinn, Estonia, 2023, pp. 1-6P	Conference	Published	10.1109/CPE-POWERENG58103.2023.10227405

5	Emiliani, A. Blinov, G. De Carne, G. Arena and D. Vinnikov, "Three Phase Four Wire High-Frequency Link Converter for Residential DC Grids," 2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Tallinn, Estonia, 2023, pp. 1-5	Conference	Published	10.1109/CPE-POWERENG58103.2023.10227416
6	G. Arena, A. Chub, M. Lukianov, R. Strzelecki, D. Vinnikov, G. De Carne, "A Comprehensive Review on DC Fast Charging Stations for Electric Vehicles: Standards, Power Conversion Technologies, Architectures, Energy Management, and Cybersecurity," *IEEE Open Journal of Power Electronics*, vol. 5, 2024, pp. 1573–1611	Journal	Published	10.1109/OJPEL.2024.3466936
7	M. Lukianov, E. R. Cadaval, G. Arena and R. Strzelecki, "Partially Isolated Multi-Active Bridge DC-DC Converter with Bidirectional EV Charging Ports," *2024 IEEE 18th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, Gdynia, Poland, 2024, pp. 1-7	Conference	Published	10.1109/CPE-POWERENG60842.2024.10604312
8	H. M. Mathew, G. Arena, A. Chub, G. De Carne, D. Vinnikov and M. Lukianov, "A Benchmark of DC-DC Converters for DC Fast Charging Stations of Electric Vehicles," *2024 9th IEEE Workshop on the Electronic Grid (eGRID)*, Santa Fe, NM, USA, 2024, pp. 1-6	Conference	Published	10.1109/eGRID62045.2024.10842879
9	Di Berardino D., Nemsow N., De Carne G. "Feasibility Assessment of Hydrogen Storage for Residential Applications: A German Neighborhood Case Study". IEEE Power and Energy Student Summit (PESS) 2025, Munich, Germany, 8–10 October 2025.	Conference Poster	Presented	N/A (poster only)
10	Khan M. A., Ebel T., et al. "Hydrogen Energy Systems for Grid Resilience and Energy Transition". Book chapter	Book contribution	Ongoing	

4. Conclusions

Work Package 3 of the SMARTGYSUM project has successfully fulfilled its primary objectives, ESRs carried out their activities by delivering considerable scientific and technological advancements in the domain of smart energy distribution, microgrids and grid of microgrids. The results of such activity is also testified by several journal paper publications and proceedings of international conferences related to WP3 topics. ESRs activities has been also devoted to the analysis of potential commercial applications of their research results, to this regard detailed business models have been formulated for each IRP. In conclusion the methodologies and prototypes developed in this work package translate advanced solutions into deployable technologies ensuring resilience and sustainability of future smart energy distribution and microgrids operation.

As concerns the PhD achievemts, ESR05 already discussed the PhD defence. ESR06 is conluding the PhD thesis and will defence on October 2026. ESR07 began his PhD in 2022 and is currently employed full-time in industry. Nevertheless, he remains an active doctoral student and is highly motivated to complete his PhD studies.
Regarding the ESR08 position, the initial researcher left the project without completing his doctoral studies. Specifically, he withdrew from the PhD at the end of 2024 to transition into a career in industry, where he is presently employed as a software developer. His successor started the PhD during the SMARTGYsum project; however, he is expected to complete the doctoral program significantly later than the project's conclusion.

A summary of the outcomes for each work package task is provided below.

Research conducted under *Task 3.1 – Energy Router for Hybrid Microgrids for efficient and robust energy and power management* has led to the successful design, modeling, and experimental validation of a novel Single-Cell Three-Phase Energy Router (SC-TP ER). This advanced power-electronic interface facilitates efficient and safe energy exchange between residential DC networks and the AC grid. Utilizing a systematic approach, the project evolved from conceptual studies to a validated hardware prototype (TRL 5), tested under various operating conditions. Key scientific contributions include a new ER topology that reduces complexity and cost, alongside novel insights into grounding and safe connection schemes. From the business perspective, the developed prototype represents a promising basis for a scalable product aimed at key stakeholders in solar energy, storage, and power electronics manufacturing. By prioritizing a hardware-centric design, the system enables the future implementation of innovative software-driven energy management, transforming the Energy Router into a smart interface for microgrid applications. These outcomes contribute significantly to the academic field of power electronics and align with European strategic goals for smart, decentralized energy infrastructures.

Research within *Task 3.2 – EV chargers, developing an active bidirectional charger able to provide anciallary services* focused on developing an active bidirectional charger providing ancillary services through a CF-MAB-based fast-charging architecture. This solution provides significant technical and economic advantages for the growing EV infrastructure market. By integrating multiple EV outputs and a high-power BES port into a single current-fed multi-active-bridge converter, the system reduces silicon area by ~25%, magnetic volume by 20–25%, and installation costs by 20–35% compared to conventional designs. These improvements stem from the CF-MAB topology's inherent strengths, including shared power paths, high-frequency isolation, and scalable multiport operation, while achieving over 96% efficiency in real-world conditions. This technology is backed by a business plan tailored to urban needs, offering lower CAPEX and seamless integration with LV DC grids. Key features include BES support for peak shaving and V2G readiness. The financial model, based on realistic BOM and competitive tender pricing, ensures a commercially viable roadmap from validated research to market-ready deployments in Europe. Rather than a simple design improvement, the CF-MAB platform paves the way for modular, high-efficiency charging infrastructure with significant long-term growth potential.

The research conducted under *Task 3.3 –Reliability and availability of Smart Transformers for cost effective and high quality of services in the grid* has led to the development of a real-time, model-assisted test bench for Modular Multilevel Converters (MMCs), which can be used in Smart Transformer applications. This platform enables safe, cost-effective, and fully dynamic testing of converter submodules under realistic operating and fault conditions, eliminating the need for a complete high-power prototype. The potential commercialization of this platform promises to enhance the safety, reliability, and performance of future Smart Transformers and renewable-based grids by providing innovative hybrid testing methodologies that bridge the gap between simulation and hardware validation. The proposed business model is focused on using the research results to become a leading provider of integrated real-time testing and validation solutions for power conversion systems, serving universities, R&D centers, and manufacturers worldwide.

Research within *Task 3.4 - Real-time modelling and validation of Distributed Energy Storage Systems and Integration strategies* focuses on DC networks, evaluating isolated versus non-isolated converter topologies regarding efficiency and short-circuit performance. To address the lack of versatile interfaces for various EV battery voltages, an 8 kW Dual Active Bridge (DAB) converter was tested across a wide output range using a bidirectional DC supply as an active load. This led to the development of a reconfigurable 400V/800V fast-charging experimental setup at KIT, maintaining high efficiency throughout its operation. Furthermore, the research extends to hydrogen-based energy storage (HES) integrated with PV in off-grid microgrids. A custom MATLAB toolchain was developed for automated system sizing and techno-economic assessment across diverse European locations. Future phases will include MATLAB/Simulink dynamic modeling and experimental validation via Power Hardware-in-the-Loop (PHIL) at the KIT Energy Lab 2.0. Despite the emerging nature of the technology, the company's consultative approach and community engagement are key to fostering trust among stakeholders. The proposed business model introduces an innovative solution to the global energy challenges faced by off-grid communities. By combining renewable energy generation with hydrogen-based storage, the company offers an environmentally sustainable and economically viable approach that ensures year-round energy availability. This dual focus on clean generation and efficient, long-term storage directly addresses a critical limitation of current renewable microgrids: the need for reliable, long-duration energy storage.

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